Simple lock–in amplifier
Rev. 5

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1 Circuit Description

This is a simple, reasonably general purpose, lock–in amplifier. The circuit has been fitted, without too much effort, to a standard euro card. It requires a triple $\pm 15V, +5V$ supply. The analog $\pm 15V$ ground (GNDA) and the digital $+5V$ (GND) are kept separate on board and should be connected together only directly at the power supplies output if good rejection of ground loops is required.

The frequency range spans from about 200 Hz to about 50kHz. It can detect the first, second and third harmonic and can use either an internal sine wave oscillator or an external frequency reference (i.e. a mechanical chopper or an external function generator). If only a fixed frequency internally generated sine wave is required the circuitry can be simplified by replacing many components with a single chip TTL quartz oscillator.

By using an external sine wave generator and only $1f$ detection the maximum operating frequency can be increased to about 150 kHz.

Since the input stage uses standard op–amps this circuit is not suitable for very low noise applications (let's say below $30\text{nV}/\sqrt{\text{Hz}}$ or $4\text{nV}/\sqrt{\text{Hz}}$ if either the high level differential input stage or the single-ended amplifier are respectively used). For better results an external preamplifier should be employed.

This document describes the Rev.5 PCB. Previous revisions are described in a similar document. The schematics for the circuit is shown in Figs.(1–3)

1.1 Clock and Reference

For generating a TTL reference signal at frequency $1f$, $2f$ or $3f$ and the sine wave output at frequency f, the starting point is a TTL oscillator generating a master clock `clk` signal at frequency $384f$. The oscillator (IC2) is the VCO section of a 74HC4046. The frequency range can be adjusted with C8 and R22. The minimum frequency can optionally be set with R20. In internal mode the oscillator and reference frequency are varied with a $10\text{k}\Omega$ variable

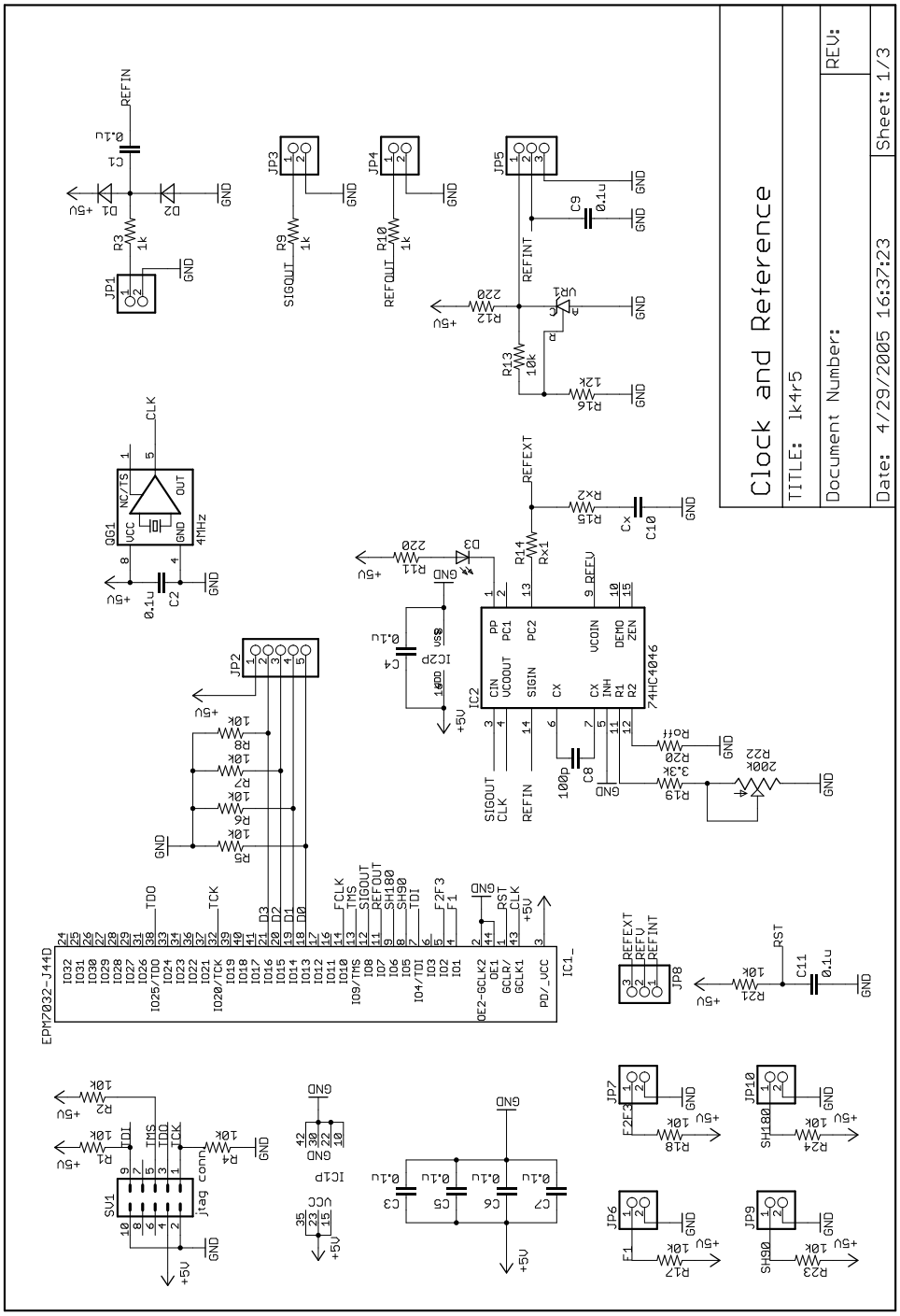

Figure 1: Schematics of the clock and reference circuit.

resistor connected at JP5, while in external mode the oscillator locks on the $384th$ harmonic of the signal coupled at JP1.

The loop filter components are C10, R14 and R15. It is difficult to design a filter with passive components that will properly operate over a frequency range of more than two decades so either mount the components on sockets or limit the locking range to a sensible range depending on your application, say from 200Hz to 1kHz for a mechanical chopper or from 10kHz to 50kHz for current modulation of a diode laser with an external oscillator. The calculation of the loop filter is described in detail in the 74HC4046 data sheet from Philips/Signetics. Choose a damping factor ζ around 1 and a natural frequency ω_n around $2\pi \times 10$Hz. The external lock condition is monitored by LED D3.

Internal/External mode is selected with JP8. The external signal is applied at JP1.

Alternatively, if only a fixed internal frequency is required, IC2 and all the related components can be replaced by a single DIL8 footprint TLL quartz oscillator, up to 20 MHz for roughly 20 MHz/384 $\simeq$ 50 kHz operation.

Using a JTAG programmable Altera MAX7000S series CLPD, the EPM7032, (IC1) some other digital signals are generated.

- The sine wave oscillator signal is generated by using a clock programmable *5th* order Butterworth filter (see later). The filter clock `fclk` is a square wave at frequency $96f$, while its input `sigout` is a square wave at frequency f.
- The reference signal `refout` is a square wave at frequency $1f, 2f$ or $3f$. A couple of switches, JP6 and JP7 are used for harmonic selection. The reference signal can also be shifted by 180 or 90 degrees by using JP9 and JP10 respectively. The 0-90 degrees range is divided in 16 parts (about 0.1 rad. resolution) by a binary coded 16 position switch connected at JP2. This resolution causes a maximum signal loss of about 0.13% on the in–phase component and is adequate for most applications even if the cancellation of the quadrature component is in general limited to 5%. A TTL logic level reference signal is available at JP3.

The verilog program (with heavy use of predefined Altera macros) for IC1 is reported below. Note that there is a small phase shift even for the 0 code.

```
// Lock in logic

module lock3(clk,rst,f1,f2f3,sh90,sh180,fclk,sigout,refout,phase);

input clk;          // main clock
input rst;          // rst
input f1,f2f3;      // 1f,2f,3f select
input sh90,sh180;   // 90 deg, 180 deg shifters
input [3:0] phase; // phase cmp input
```

```
output fclk;              // filter clock
output sigout,refout;     // signal and reference outputs

//reset logic
reg reset;
wire [4:0] stin;
reg [4:0] stout;
wire stcp;

assign stin[3:0]=phase;
assign stin[4]=sh90;

//latch status
always@(posedge clk or negedge rst)
   if(rst==0)
     stout=0;
   else
     stout=stin;

//status comparator
lpm_compare stcmp (.dataa(stin), .datab(stout), .aneb(stcp));
defparam stcmp.lpm_width = 5;

//reset ff
always@(negedge clk or negedge rst or posedge stcp)
   if(rst==0 )
     reset=1;
   else if(stcp==1)
          reset=1;
        else
          reset=0;

//signal counter
wire clk2,clk3,clk4,clk6,sigck0;
assign fclk=clk4;

lpm_counter div4a (.clock(clk), .aclr(reset), .q(clk2));
defparam div4a.lpm_width = 2;

lpm_counter div4b (.clock(clk), .clk_en(clk2), .aclr(reset), .q(clk4));
defparam div4b.lpm_width = 2;

lpm_counter div3 (.clock(clk), .aclr(reset), .cout(clk3));
defparam div3.lpm_width = 2,
         div3.lpm_modulus = 3;
```

```
lpm_counter div2 (.clock(clk), .clk_en(clk3), .aclr(reset), .cout(clk6));
defparam div2.lpm_width = 1;

lpm_counter sigc0 (.clock(clk), .clk_en(clk2 & clk4),.aclr(reset),
                   .cout(sigck0));
defparam sigc0.lpm_width = 6,
         sigc0.lpm_modulus = 48;

lpm_counter sigc1 (.clock(clk), .clk_en(sigck0 & clk4 & clk2), .aclr(reset),
                   .q(sigout));
defparam sigc1.lpm_width = 1;

//reference counter

//multiplexer
wire refck0;
wire [3:0] ckmux;
wire [1:0] fsel;

assign fsel[1]=f1;
assign fsel[0]=f2f3;

assign ckmux[0]=clk6 & clk3;
assign ckmux[1]=clk3;
assign ckmux[2]=clk2;
assign ckmux[3]=clk6 & clk3;

mux mux1 (.data(ckmux), .sel(fsel), .result(refck0));
defparam mux1.width = 4;
defparam mux1.widths = 2;

//Half rotation counter
wire [4:0] qr0;
wire dcmp,qr1;
reg cmp;

lpm_counter refc0 (.clock(clk), .clk_en(refck0), .aclr(reset), .q(qr0));
defparam refc0.lpm_width = 5;

lpm_compare phasecmp (.dataa(qr0), .datab(stout), .aeb(dcmp));
defparam phasecmp.lpm_width = 5;

always@(negedge clk or posedge reset)
   if(reset==1)
     cmp=0;
   else
```

```
    cmp=dcmp;

lpm_counter refc1 (.clock(cmp), .aclr(reset), .q(qr1));
defparam refc1.lpm_width = 1;

// invert refout when sh180 or f2
assign refout=qr1^sh180^(f1 | !f2f3);
endmodule
```

Pin connections for IC1 are shown in Tab.1

signal	pin
clk	43
fclk	14
refout	11
sigout	12
f1	4
f2f3	5
sh90	8
sh180	9
phase0	18
phase1	19
phase2	20
phase3	21
rst	1

Table 1: Connection table for the CPLD.

1.2 Oscillator

The sine wave for the internal oscillator is generated using a LTC1063, a clock programmable $5th$ order Butterworth filter (IC3). The -3dB corner frequency fc is set at 1/100 the clock frequency. Since the input signal is a square wave at 1/96 the clock frequency, i.e. $1.04fc$, the fundamental is attenuated by less than 6 dB, while the third harmonic, at $3.13fc$ is attenuated by about 55 dB. The input square wave is attenuated (around 2.5V) to reduce harmonic distortion by the network formed by D4,R25,R28 and R30. The output is filtered by the inverting amplifier formed by IC4 (LTC1152 or any single supply, rail–to–rail low distorsion audio amplifier) with a variable attenuation provided by a 100kΩ pot. connected to JP11 . The DC component is finally removed by C13 and the output is available at `JP12`

1.3 Input Amplifier

For the input amplifier two choices are available.

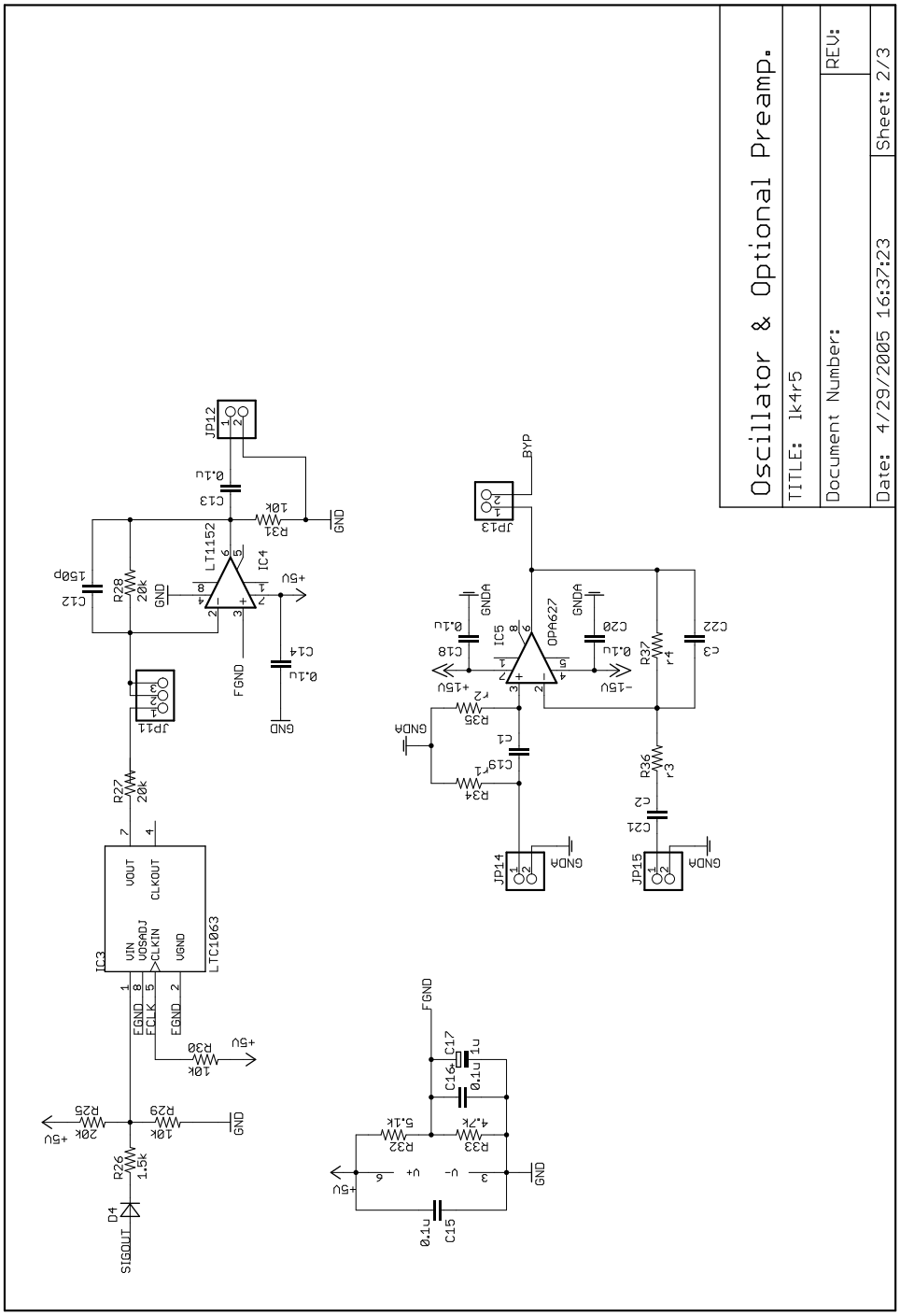

Figure 2: Schematics of the sinusoidal oscillator and optional preamplifier.

In the first case, which should be the preferred choice, the input amplifier uses a differential buffer (IC8) and an AC coupled gain stage (IC6). IC6 can have a gain of 3,10,30 or 100. Note that a gain–bandwidth product of at least 16MHz is required for $3f$ operation at maximum gain and frequency. The bandwidth of IC6 is set at low frequency by C25 and R39 (160 Hz). High frequency (gain dependent) bandwidth limiting can be achieved with C30. The input connector is JP17.

Alternatively, if a single ended input stage is acceptable, it is possible to omit IC8 and use IC5. It is possible to configure IC5 as an inverting or noninverting AC or DC coupled voltage or transimpedance amplifier with input at `JP14` or `JP15` by assembling only the required components. The output of IC5 can then be connected at the input of IC6 via `JP13`

1.4 Demodulator and Output

The demodulator is a classic AD630 (IC7) set for gain $G = 2$. IC7 operates as a $\pm G$ amplifier where the sign of G is selected by that of the reference input.

To adjust the gain and offset of IC7 R45 and R48 are provided. With the input shorted the output of the demodulator will be a small amplitude square wave: use R48 to minimize the amplitude then R45 to move the DC offset to zero.

The time constant is set by R40,R54 and C24,C28,C32,C33 and C34 (from 10μs to 0.1 s in $\times 10$ steps) and selected with a rotary switch connected to `JP16` driving four analog switches in IC9.

IC10 is a gain $G = -1$ buffer to avoid loading the filter. Adjust R53 if you need a different gain. The lock–in output is available at `JP19`. If necessary, a pot. on the front panel connected as a voltage divider can be used as variable attenuator.

The silkscreen for the circuit is shown in Fig.(4) while the part list is given in table below

Part list for the lock–in amplifier

Qty	Value	Parts	Notes
1	EPM7032	IC1	Altera MAX7000S CPLD
1	74HC4046	IC2	VCO+PFD
1	LT1063	IC3	Switched capacitors filter
1	LTC1152	IC4	
3	OPA627	IC5–6,IC10	Or similar precision Op. Amp.
1	AD630	IC7	Demodulator
1	AMP03	IC8	Differential Amp.
1	ADG441	IC9	Quad. Analog Switch
1	TL431	VR1	Or similar 2.5V Voltage Reference
1	4MHz	QG1	TTL quartz Osc., see text

Qty	Value	Parts	Notes
22	10kΩ	R1–2,R4–8,R13, R17–18,R21,R23–24, R29–31,R41,R43–44, R47,R50–51	
5	1kΩ	R3,R9–10,R38–39	
2	220Ω	R11–12	
1	Rx1	R14	PLL loop filter, see text
1	Rx2	R15	PLL loop filter, see text
1	12kΩ	R16	
1	3.3kΩ	R19	
1	Roff	R20	see text
4	20kΩ	R25,R27–28,R42	
1	1.5kΩ	R26	
1	5.1kΩ	R32	
1	4.7kΩ	R33	
1	r1	R34	see text
1	r2	R35	see text
1	r3	R36	see text
1	r4	R37	see text
3	200kΩ	R40,R53–54	
2	100kΩ	R46,R56	
1	30kΩ	R49	
1	3kΩ	R52	
1	100Ω R55		
1	200kΩ R22	10 turns trimmer	
2	10kΩ R45,R48	10 turns trimmer	
1	10kΩ JP5	10 turns pot.; f. panel	
1	100kΩ JP11	10 turns pot.; f. panel	
30	0.1μF	C1–7,C9,C11,C13–16, C18,C20,C23, C26–29,C31,C36, C38–41,C43–44,C46–47	
2	100pF	C8,C34	
1	Cx	C10	PLL loop filter, see text
1	150pF	C12	
1	c1	C19	see text
1	c2	C21	see text
1	c3	C22	see text
2	1μF C24–25		
1	Cx	C30	Input filter, see text
1	10nF	C32	
1	1nF	C33	
1	27pF	C35	
1	1μF C17		

Qty	Value	Parts	Notes
3	47μF	C37,C42,C45	
3	1N4148	D1–2,D4	
1	LED	D3	
3	vk200	L1–3	
1	H15ML	X1	15 Poles DIN41612 male conn.
1	ML10	SV1	JTAG programming connector
1	HEX1	JP2	Hex. coded 16 pos. switch; f. panel
5	SPDT	JP6–10,	SPDT switches; f. panel
2	4x1 sw.	JP16,JP18	4 ways to 1; f. panel

2 Expected performances

This design is mainly intended to lock diode lasers for MOTs etc. on saturation signals from a cell and save good instruments for serious applications. It is meant to be reasonably cheap and simple to assemble. Nevertheless it can be adapted to more demanding applications so it is worth discussing its expected performances when inserted in a feedback loop. The output noise level can be described at short times with a noise spectral density and at long ones with an output voltage drift, mainly induced by temperature changes. The input stages before the demodulator contribute to the total noise only with their noise density close to the reference frequency. By choosing a reference frequency above 1 kHz it is safe to assume that their $1/f$ noise can be neglected. IC8 has a noise density close to $20\text{nV}/\sqrt{\text{Hz}}$, probably acceptable for a high level input. For IC6 a low noise unit with characteristics close to those of the OPA627 will have a density close to $5\text{nV}/\sqrt{\text{Hz}}$, comparable with the Johnson noise of R39. If the single ended input stage with IC5 is used instead of IC6 just be sure that the gain is high enough. If the signal is coming from a photodiode it should be easy to be shot–noise limted with just a simple external transimpedance amplifier. After demodulation the noise is dominated by the output noise of IC7, measured at $120\text{nV}/\sqrt{\text{Hz}}$. The minimum combined gain of IC6 and IC7 is 6 so this translates to some $20\text{nV}/\sqrt{\text{Hz}}$ referred to IC6 input. IC7 and IC10 will contribute instead to $1/f$ noise. The corner should be certainly below 100 Hz.

Long term stability due to temperature changes will be dominated by the 2 ppm/C$^\circ$ ΔG coefficient of IC7 and the V_{off} thermal coefficient of IC10, in the 1 μV/C$^\circ$ range for a precision unit.

If the output voltage is around few Volts it should be possible to have an output stability between 2 and 5 ppm/C$^\circ$. A significant stability improvement will probably require replacing IC7.

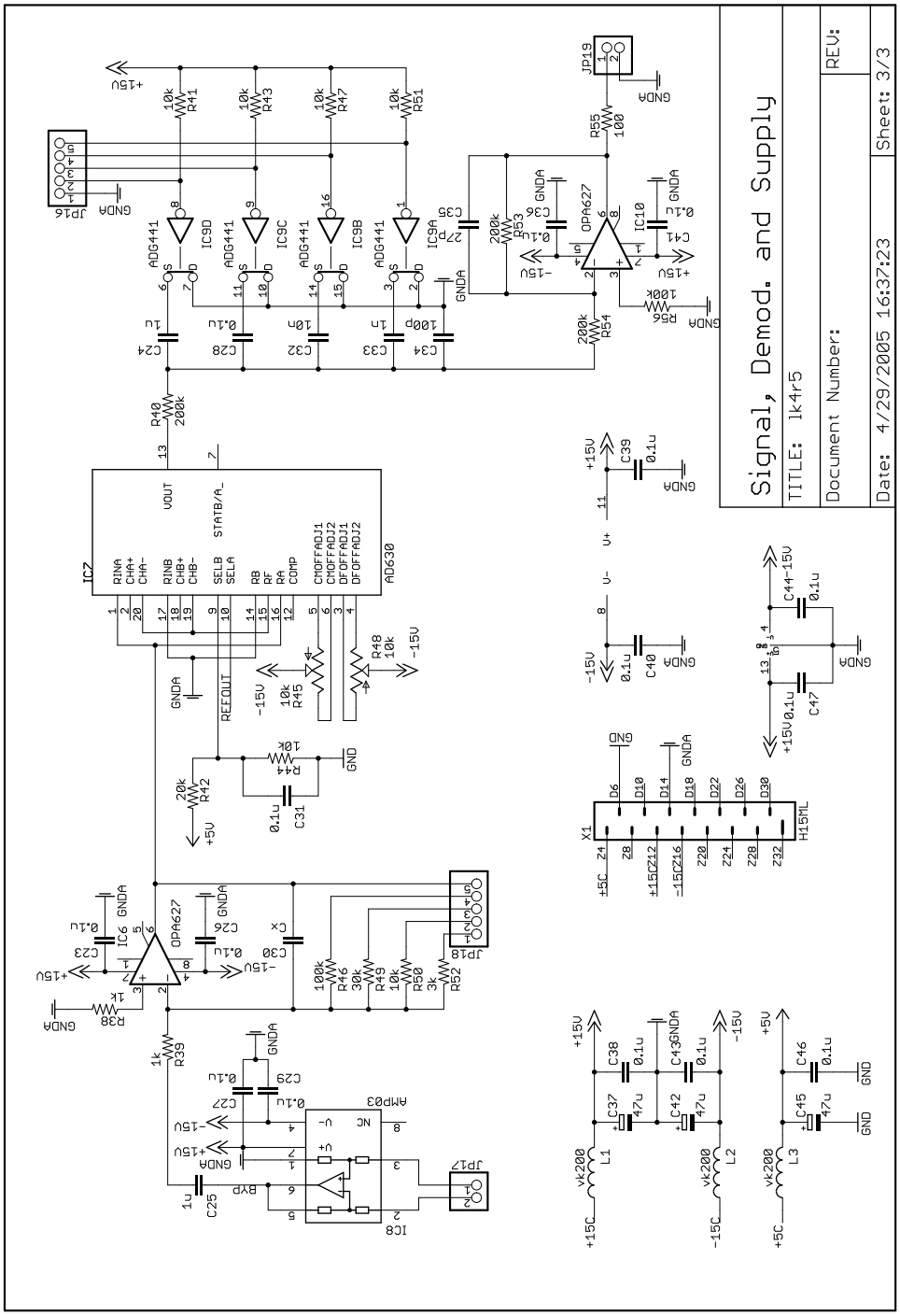

Figure 3: Schematics of the input amplifier and demodulator.

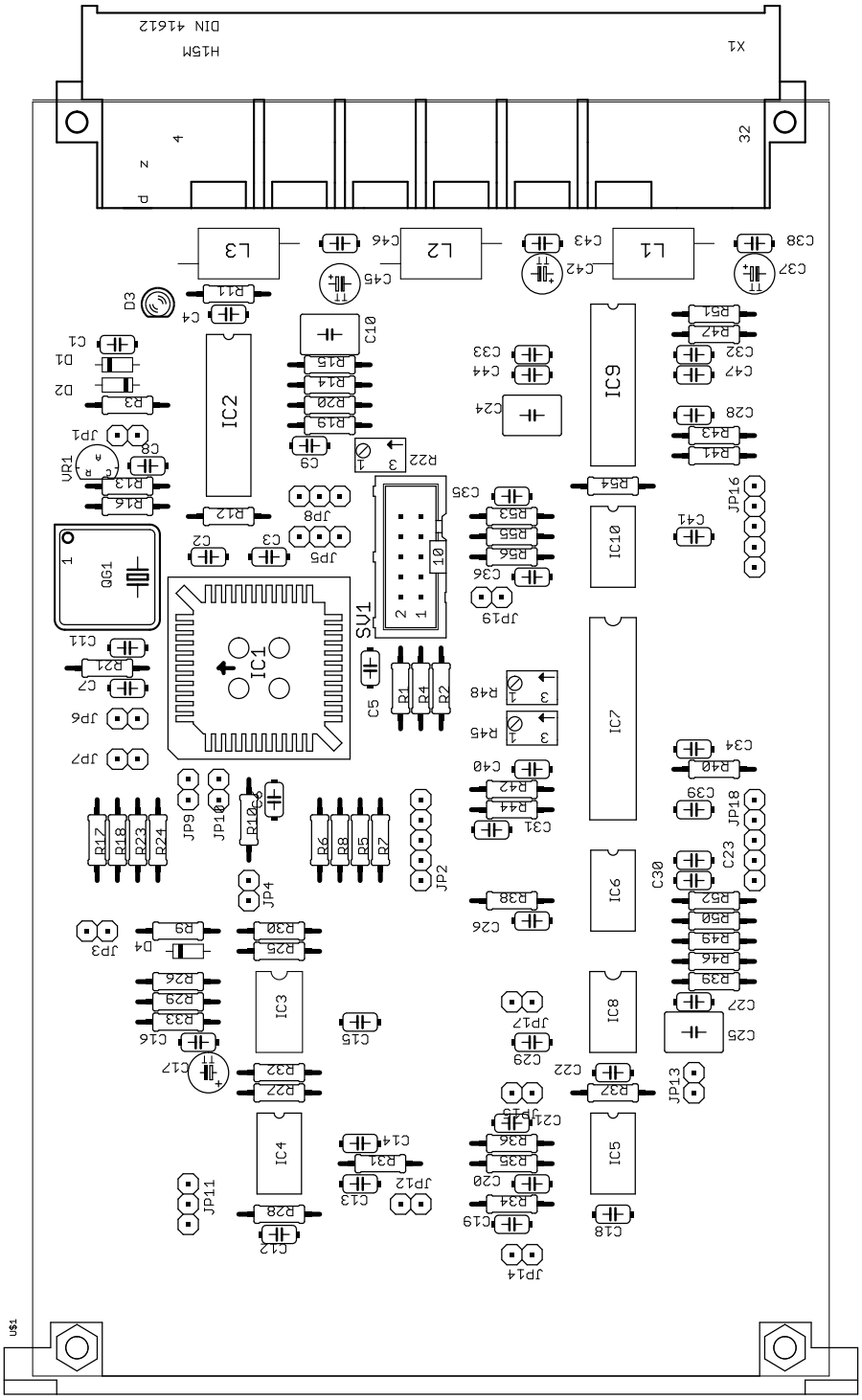

Figure 4: Silkscreen for the lock–in board.