CMOS Phase-Locked-Loop Applications Using the CD54/74HC/HCT4046A and CD54/74HC/HCT7046A

W. M. Austin *Standard Linear & Logic*

ABSTRACT

Applications of the HC/HCT4046A phase-locked loop (PLL) and HC/HCT7046A PLL with lock detection are provided, including design examples with calculated and measured results. Features of these devices relative to phase comparators, lock indicators, voltage-controlled oscillators (VCOs), and filter design are presented.

Contents

List of Figures

List of Tables

Introduction

This application report provides the circuit designer with information on the use of the HC/HCT4046A† phase-locked loop (PLL) devices with a voltage-controlled oscillator (VCO) and the HC/HCT7046A‡ PLL devices with in-lock detection in phase-locked circuits. A description of the basic loop operation is included as an introduction to phase-lock techniques. Complete circuit designs, with and without a frequency-divide ratio, are included as examples. Examples also are given of various filters operating over a range of frequencies.

Basic Loop Operation

The HC/HCT4046A PLL with VCO is a high-speed CMOS IC designed for use in general-purpose PLL applications, including frequency modulation, demodulation, discrimination, synthesis, and multiplication. Specific applications include data synchronizing, conditioning and tone decoding, as well as direct VCO use for voltage-to-frequency conversion and speed-control applications.

The IC contains a VCO and a choice of phase comparators (PCs) for support of the basic PLL circuit, as shown in Figure 1. The low-pass filter (LPF) is an essential part of the loop and is needed to suppress noise and high-frequency components. An optional fourth part of the loop is the divide-by-N frequency divider, which is needed when the VCO is run at a multiple of the signal-input reference frequency. To facilitate support of a variety of general-purpose applications, both the filter and divider are external to the HC/HCT4046A. These and other aspects of the application of the HC/HCT4046A are explained in the following paragraphs through a variety of loop-design examples.

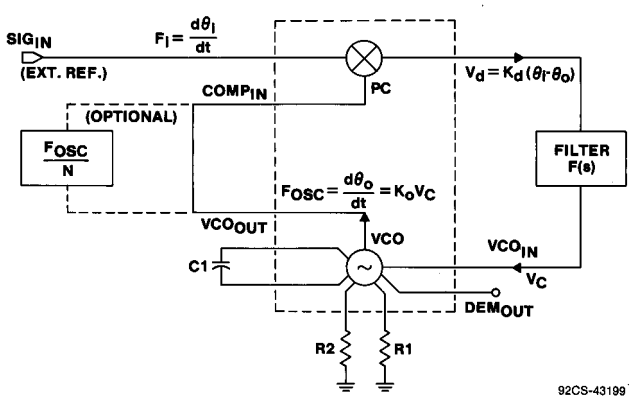


Figure 1. Block Diagram of an HC/HCT4046A in a Typical PLL Circuit

† HC/HCT4046A refers to the CD54HC4046A, CD74HC4046A, CD54HCT4046A, and CD74HCT4046A devices.
‡ HC/HCT7046A refers to the CD54HC7046A, CD74HC7046A, CD54HCT7046A, and CD74HCT7046A devices.

For a full treatment of PLL theory, the reader is directed to the *Bibliography and References,* section where there are a number of references that support the descriptions and explanations given in this application report. The symbols and terminology used in this application report primarily follow the book, *Phase-Lock Techniques.*[1] The details of derivations of the equations can be found in the references.

Some understanding of feedback theory as a background for designing PLL circuits is helpful, but lack of this understanding should not be a deterrent to anyone choosing to apply the HC/HCT4046A in relatively simple, second-order PLL circuits. The purpose of this application report is to present a solid tutorial on CMOS PLL techniques, including extensive information on the VCO characteristics. A designer then can apply the information to a variety of circuit applications.

Before beginning to apply the HC/HCT4046A in PLL circuits, a designer should have an understanding of the parameters and equations used to define loop performance. Furthermore, the designer should recognize that PLL circuits are a special case of feedback systems. Where servomechanism feedback systems primarily are concerned with position control, PLL feedback systems primarily are concerned with the phase and tracking of a VCO relative to a reference signal input. While a phase error can be anticipated, no differential in frequency is desired after phase lock is established. General feedback theory is applied in PLL use just as it is in servomechanism systems. Some of the symbols and terminology used to describe PLL systems were borrowed from servo systems, giving rise to such terms as damping factor, natural loop resonant frequency, and loop bandwidth.

Description of the HC/HCT4046A

The block diagram of the HC/HCT4046A (see Figure 2) shows the least complex form of external loop filtering. In addition to the VCO, the HC/HCT4046A provides a choice of three phase comparators. The HC/HCT7046A is an equivalent device, differing only in the tradeoff of a third phase comparator (PC3) for a lock detector (LD). The pinouts of the HC/HCT4046A and HC/HCT7046A differ in a minor way from that of the earlier CMOS PLL-type CD4046B, which differs functionally in that it has a zener reference diode in place of PC3 or the lock detector.

Unless otherwise noted in the following information, all descriptions and operational references apply to the HC/HCT4046A and the HC/HCT7046A.

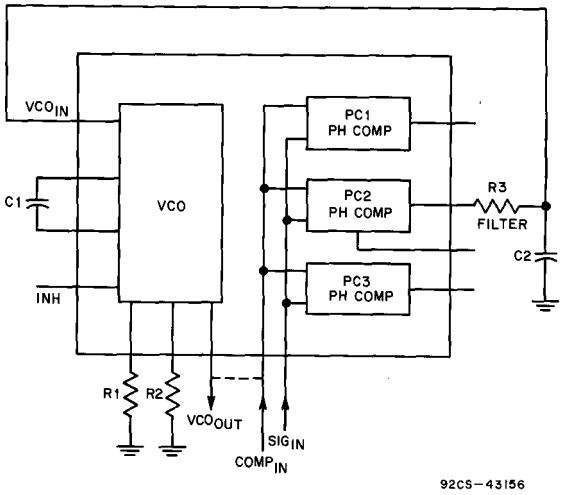


Figure 2. Block Diagram of an HC/HCT4046A With External Loop Filtering

Figures 3 and 4 show the HC/HCT4046A and HC/HCT7046A functional block diagrams, respectively. The VCO of the HC/HCT4046A is identical to that of the HC/HCT7046A and has the same operating characteristics. The HCT versions of these oscillator circuits differ from the HC versions by having TTL logic levels at the inhibit inputs. Improved linear differential amplifiers are used to control the current bias established by resistors R_1 and R_2; amplifying current mirrors control the charge rate of the timing capacitor C_1. Descriptive and design information on frequency control of the VCO is given in the following sections.

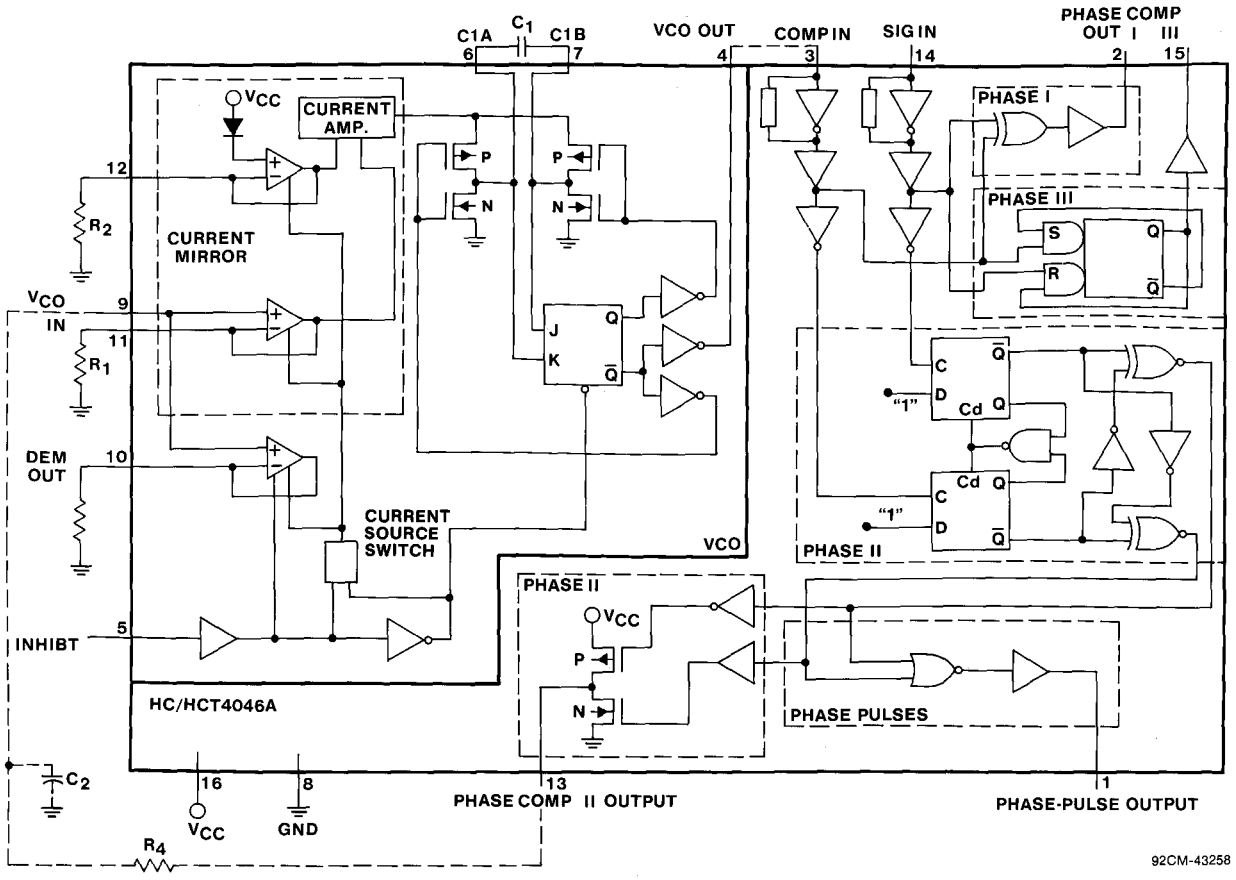


Figure 3. HC/HCT4046A Functional Block Diagram

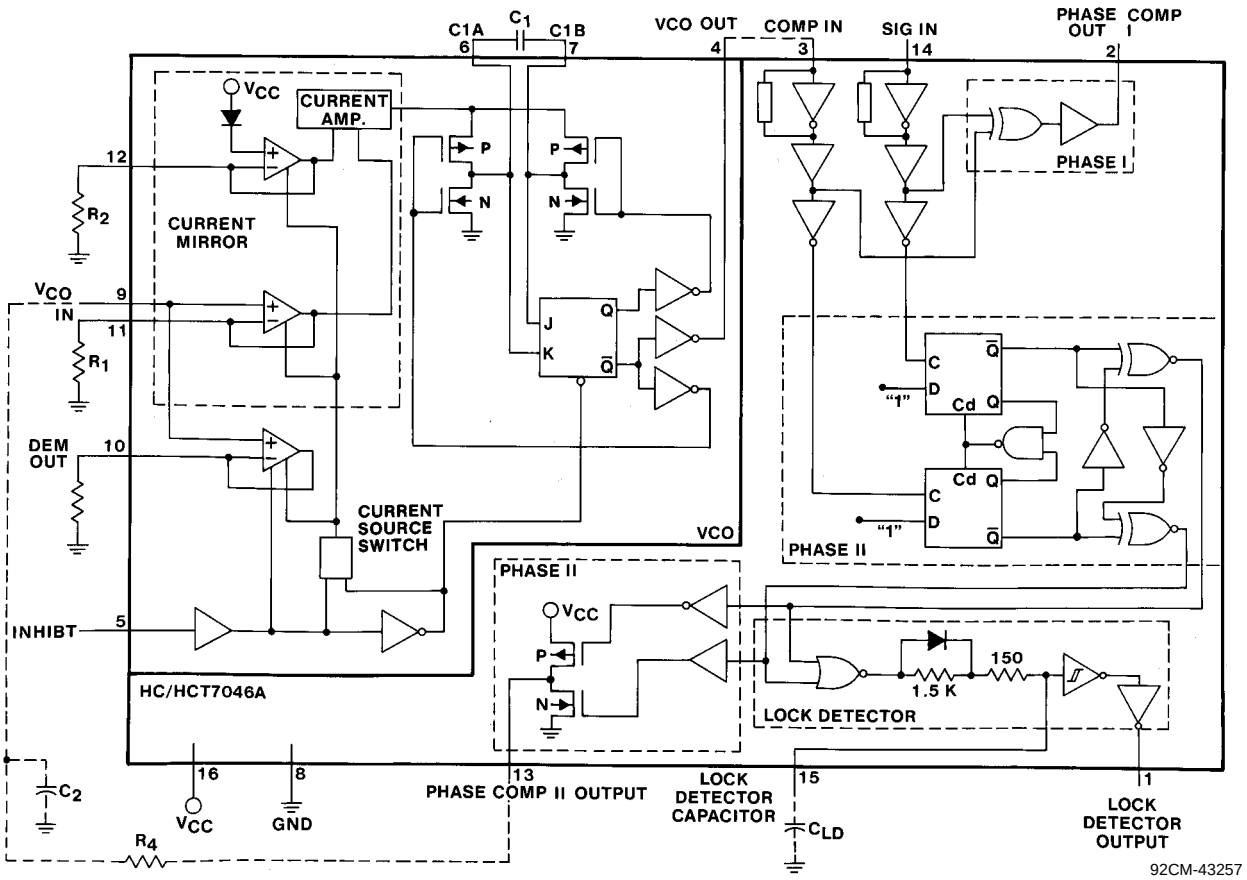


Figure 4. HC/HCT7046A Functional Block Diagram

Phase Comparators (PCs)

While there are many types of PCs (also referred to as detectors), the ones chosen for the CMOS PLL design are based on accepted industry-standard types. The choice also was based on design flexibility and the compatibility of CMOS technology with PC applications. Figure 3 shows the logic diagram of the phase-comparator circuit with PC1 (PHASE I), PC2 (PHASE II), and PC3 (PHASE III) identified. The comparators consist of an exclusive OR (PC1), an edge-triggered J-K flip-flop (PC2), and an edge-triggered R-S flip-flop (PC3). The phase-comparator inputs are in parallel, making the user's choice a matter of selecting the pinout to the preferred PC.

Both the external-reference signal input and the comparator input are internally self biased to $V_{DD}/2$ to permit ac coupling from the drive signal sources. When ac-coupled input signals are used, the drive sensitivity typically is better than 50 mV_{pp}. The comparator input normally is used for the VCO direct-coupled input; however, the comparator section is independent of the VCO for stand-alone use.

The signals to both phase-comparator inputs are amplified with limiting that ignores amplitude changes. With respect to the HC4046A versus the HCT4046A, only the inhibit input levels are different; the drive levels for the phase-comparator inputs are the same. When TTL drive levels are used for the signal input to the detectors, either ac coupling or TTL-to-CMOS level conversion should be used to correctly drive the $V_{DD}/2$ switch level. Where the signal-input source voltage is less than the logic level in peak-to-peak amplitude, ac coupling is necessary. In addition, ac coupling is preferred, with reduced-drive signals to minimize transient switching and harmonic interference with the VCO.

Appendix I provides a summary of the phase-comparator options. An extended description of the three phase comparators is in the following sections.

Operation of Phase Comparator PC1

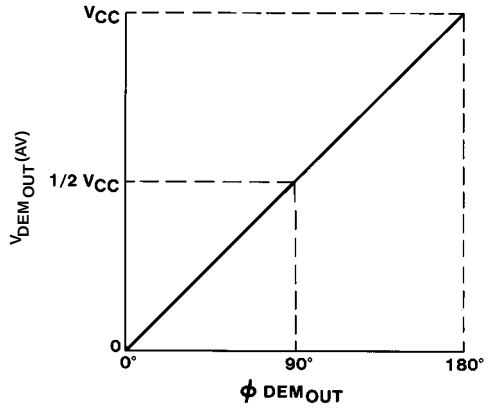
PC1 is an exclusive-OR logic circuit. The signal and comparator input frequencies (f_i) must have a 50% duty factor for the maximum locking range to be obtained. The transfer characteristic of PC1, assuming the ripple frequency ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMout} = (V_{CC}/\pi)(\phi\ SIG_{in} - \phi\ COMP_{in}) = V_{PC1out}$$

Where:

V_{DEMout} is the demodulator output at pin 10 and equals V_{PC1out} via the LPF.
ϕ is the phase angle in degrees.

The average output voltage from PC1, fed to the VCO input via the LPF and seen at the demodulator output at pin 10, is the resultant of the phase differences of signals (SIG_{in}) and the comparator input ($COMP_{in}$) (see Figure 5). The average of V_{DEMout} is equal to $V_{CC}/2$ when there is no signal or noise at SIG_{in} and, with this input, the VCO oscillates at the center frequency (f_o). Typical waveforms for the PC1 loop, locked at f_o, are shown in Figure 6.



$V_{DEMout} = V_{PC1out} = (V_{CC}/\pi)\ (\phi SIG_{in} - \phi COMP_{in})$
$\phi DEMout = (\phi SIGin - \phi COMPin)$

Figure 5. PC1 Average Output Voltage as a Function of Input Phase Difference

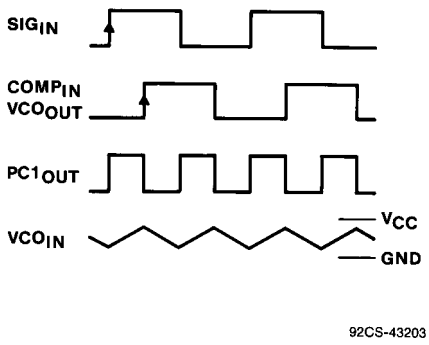


Figure 6. Typical Waveforms for PLL With PC1 Loop Locked at f_o

The frequency-capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock for initially out-of-lock conditions. The frequency lock range($2f_l$) is defined as the frequency range of input signals on which the locked loop will remain in lock. The capture range is smaller or equal to the lock range. The capture range of PC1 depends on the LPF characteristics and can be made as large as the lock range. This configuration retains lock behavior even with very noisy signal input. PC1 can lock to input frequencies within the locking range of VCO harmonics.

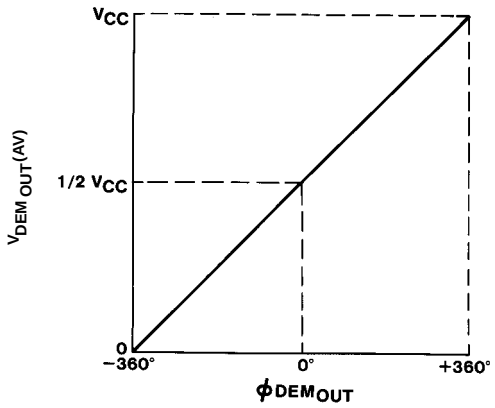
Operation of Phase Comparator PC2

For most applications, the features of PC2 provide the most advantages. It is a positive-edge-triggered phase and frequency detector. When the PLL uses this comparator, the loop is controlled by positive signal transitions, and control of the duty factor of SIG_{in} and $COMP_{in}$ is not required. PC2 is composed of two D-type flip-flops and a 3-state output stage and has controlled gating. The circuit functions as an up-down counter, where SIG_{in} causes an up count and $COMP_{in}$ causes a down count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMout} = (V_{CC}/4\pi)(\phi\ SIG_{in} - \phi\ COMP_{in}) = V_{PC2out}$
or
$V_{DEMout} = (V_{CC}/2\pi)(\phi\ SIG_{in} - \phi\ COMP_{in}) = V_{PC2out}$ (see Appendix B)

where PC2 gain is mode dependent.

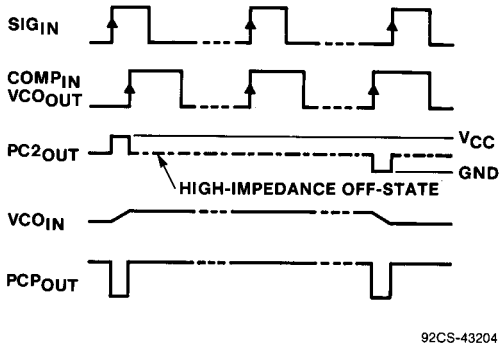
The average output voltage from PC2, fed to the VCO via the LPF and seen at the demodulator output at pin 10, is the resultant of the phase differences of SIG_{in} and $COMP_{in}$ (see Figure 7). Typical waveforms for the PC2 loop, locked at f_o, are shown in Figure 8.



$V_{DEMout} = V_{PC2out} = (V_{cc}/4\pi)\ (\phi SIGin - \phi COMPin)$
$\phi_{DEMout} = (\phi SIGin - \phi COMPin)$

92CS-43201

Figure 7. PC2 Average Output Voltage as a Function of Input Phase Difference



92CS-43204

Figure 8. Typical Waveforms for PLL With PC2 Loop Locked at f_o

When the frequencies of SIG_{in} and $COMP_{in}$ are equal but the phase of SIG_{in} leads that of $COMP_{in}$, the PMOS device at the PC2 output (see Figures 3 and 4) is held on for a time corresponding to the phase difference. When the phase of SIG_{in} lags that of $COMP_{in}$, the NMOS device is held on. When the frequency of SIG_{in} is higher than that of $COMP_{in}$, the PMOS device is held on for a greater portion of the signal cycle time. For most of the remainder of the cycle time, the NMOS and PMOS devices are off (3-state). If the SIG_{in} frequency is lower than the $COMP_{in}$ frequency, it is the NMOS device that is held on for most of the cycle.

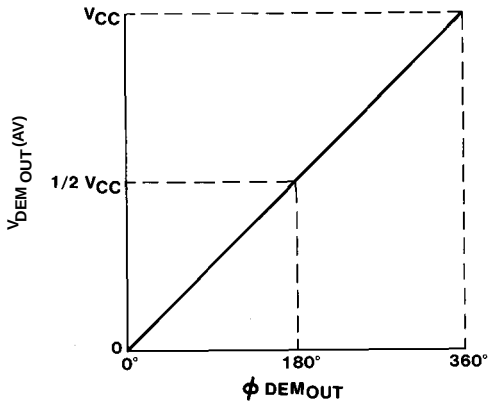
As locked conditions are achieved, the filtered output voltage from PC2 corrects the VCO until the comparator input signals are phase locked. Under stable phase-locked conditions, the VCO input voltage from the output of the LPF is constant, and the PC2 output is in a 3-state condition.

Operation of Phase Comparator PC3 (HC/HCT4046A Only)

The circuit of PC3 is a positive-edge-triggered sequential phase detector that uses an R-S flip-flop. When PC3 is used as the PLL phase comparator, the loop is controlled by positive signal transitions. This type of detector is not sensitive to the duty factor of SIG_{in} and $COMP_{in}$. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMout} = (V_{CC}/2\pi)(\phi\ SIG_{in} - \phi\ COMP_{in}) = V_{PC3out}$ via the LPF

The average output from PC3, fed to the VCO via the LPF and seen at the demodulator output, is the resultant of the phase differences of SIG_{in} and $COMP_{in}$ (see Figure 9). The typical waveforms for the PC3 loop, locked at f_o, are shown in Figure 10.



$V_{DEMout} = C3out = (V_{cc}/2\pi)\ (\phi SIGin - \phi COMPin)$
$\phi DEMout = (\phi SIGin - \phi COMPin)$

Figure 9. PC3 Average Output Voltage as a Function of Input Phase Differences

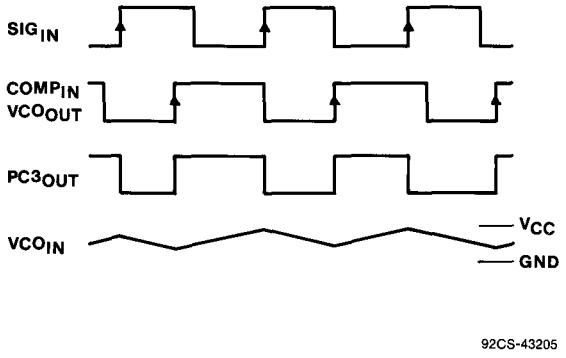


Figure 10. Typical Waveforms for PLL With PC3 Loop Locked at f_o

The phase characteristics of PC3 differ from those of PC2 in that the phase angle between SIG_{in} and $COMP_{in}$ in PC3 varies between 0 and 360 degrees and is 180 degrees at the center frequency. PC3 also has a greater voltage swing than PC2 for the same input phase differences. While the conversion gain may be higher in PC2, PC3 produces a higher ripple content in the VCO or $COMP_{in}$ signal.

Lock Indicators

PCP_{out} of the HC/HCT4046A

Although the phase-comparator pulse output (PCP_{out}) is shown as part of PC2 in Figure 8, the phase indication is present when either PC1, PC2, or PC3 is used. The PCP_{out} phase-lock condition is present because the inputs for SIG_{in} and $COMP_{in}$ are in parallel. As noted in the waveforms of Figure 8, PCP_{out} at pin 1 of the HC/HCT4046A remains in the high state when the loop is phase locked. When either the PMOS or NMOS device is on, the PCP_{out} is low. How the PCP_{out} is used depends on the application. To fully utilize this output as a practical lock indicator, a smoothing filter is needed to reduce the effects of noise and marginal lock-on flicker.

Lock Detector of the HC/HCT7046A

Additional lock-indicator circuitry has been added to the HC/HCT7046A, replacing the PC3 function with an improved lock detector and filter. As shown in the logic diagram for the HC/HCT7046A in Figure 4, the PC2 circuit provides the same set of indicator signals as the PCP_{out} circuit of the HC/HCT4046A shown in Figure 3. Additional stages are used to process the lock-detection (LD) output signal of the HC/HCT7046A.

Detection of a locked condition is accomplished in the HC/HCT7046A with a NOR gate and an envelope detector (see Figure 11). When the loop is phase locked, the output of the NOR gate is high and the lock detector output (pin 1) is at a constant high level. As the loop tracks the SIG_{in} on pin 14, the NOR gate generates pulses having widths that represent the phase difference between the $COMP_{in}$ (from the VCO) and SIG_{in}. The time between pulses is approximately equal to the time constant (T) of the VCO center frequency. During the rise time of the pulse, the diode across the 1.5-kΩ resistor is forward biased, and the time constant in the path that charges the lock-detector capacitor (C_{LD}) is given by:

$T = (150\ \Omega \times C_{LD})$

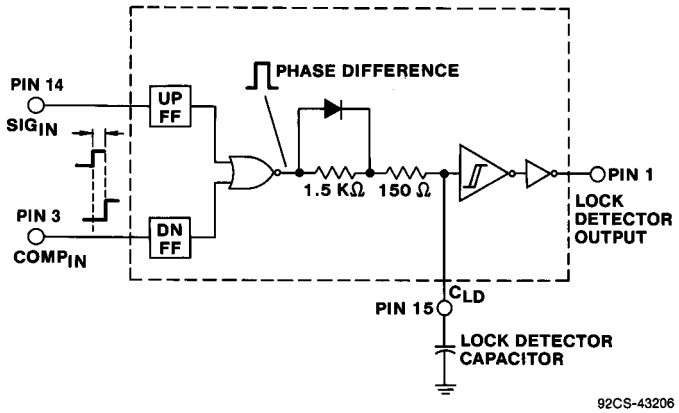


Figure 11. Lock-Detector Circuitry in the HC/HCT7046A

The discharge circuit includes the 1.5-kΩ resistor. The capacitor waveform is a sawtooth (see Figure 12). The lock-detector capacitor value is determined by the center frequency of the VCO. The typical range of capacitance for a frequency of 10 MHz is about 10 pF, and for a frequency of 100 kHz, about 1000 pF. The value of C_{LD} can be selected by using the graph in Figure 13. As long as the loop remains locked and tracking, the level of the sawtooth does not go below the switching threshold of the Schmitt-trigger inverter. If the loop breaks lock, the width of the error pulse is wide enough to allow the sawtooth waveform to go below the threshold, and a level change at the output of the Schmitt-trigger indicates a loss of lock (see Figure 14). The lock-detector capacitor also filters out small glitches that can occur when the loop is either seeking or losing lock.

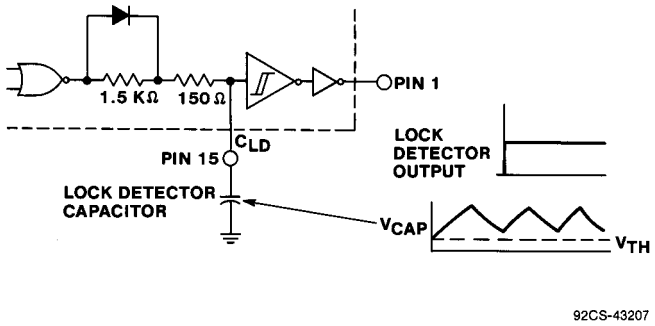


Figure 12. Waveform at Lock-Detector Capacitor When in Lock

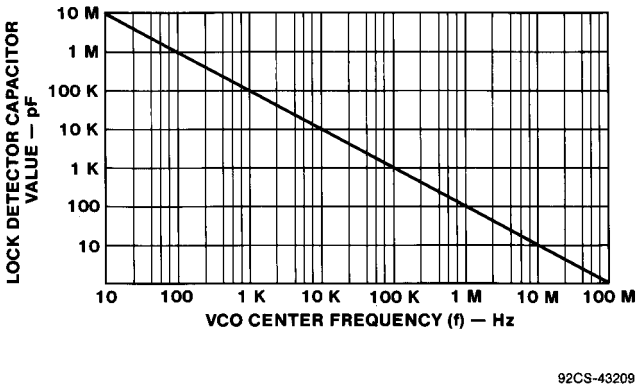


Figure 13. Graph For Determining Value of Lock-Detector Capacitor

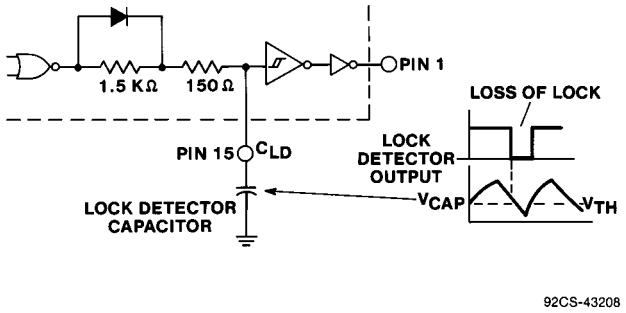


Figure 14. Waveforms at Lock-Detector Capacitor When Unlocked

As noted for PCP_{out} of the HC/HCT4046A, the lock-detector function of the HC/HCT4046A is present in any application of PC1, PC2, or PC3. However, it is important to note that, for applications using PC1, the lock detector indicates only a locked condition on the fundamental frequency and not on the harmonics that PC1 may lock on. If lock detection is needed for the harmonic locking range of PC1, the lock-detector output must be ORed with the output of PC1.

Voltage-Controlled Oscillator (VCO)

The high-speed CMOS PLL ICs incorporate a versatile and easy-to-use VCO with a number of enhanced features, resulting from the high-speed CMOS process. The most notable advantage is an order-of-magnitude increase in the VCO frequency range over that of the CD4046B.

The following VCO applications are intended to highlight problem solutions. Equations for the VCO frequency have been developed with emphasis on the high-frequency range. Graphical comparisons of measured and calculated frequency results are given.

VCO Description

Figure 15 shows a functional diagram of the VCO control circuit of the HC/HCT4046A. The frequency and offset frequency amplifiers are configured to convert voltage to current, which is then amplified in the current-mirror-amplifier(CMA) blocks before being summed. The summed current is directed to the oscillator section consisting of inverters G_1 and G_2. The inverters, switching as H drivers, control charge and discharge current to the oscillator range capacitor, C_1. The oscillator loop consists of flip-flop FF with feedback from the cross-coupled outputs to G_1 and G_2.The demodulator output amplifier can be used optionally to buffer the filtered output of the phase comparator. In normal use, the load resistors are in the range of 50 kΩ to 100 kΩ. An inhibit amplifier controls the oscillator and CMA circuits. The output from one side of the flip-flop is buffered and output to the VCO_{out} at pin 4.

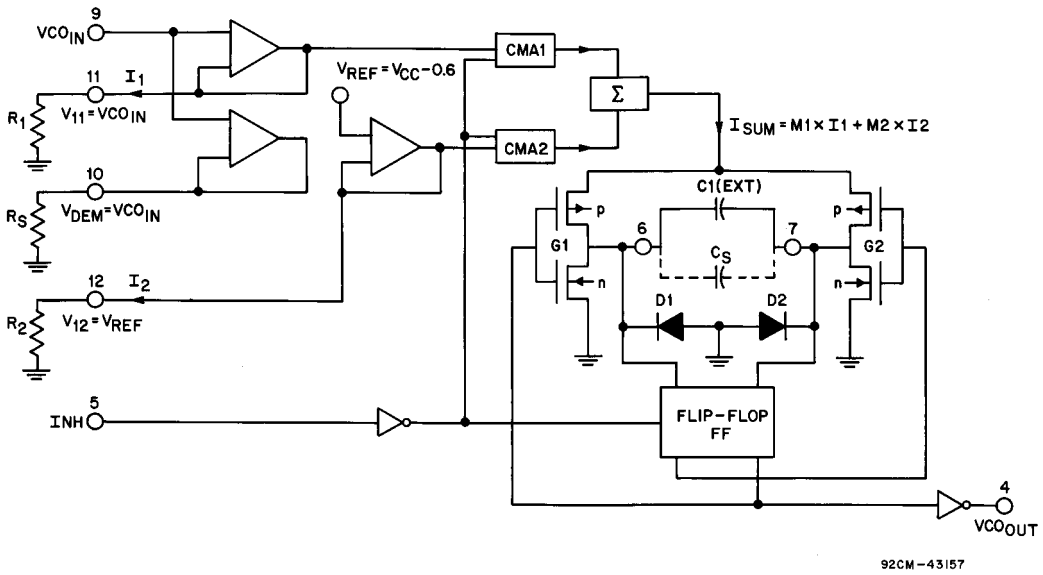


Figure 15. VCO Portion of CD74HC4046A/7046A Functional Block Diagram

The external components R_1, R_2, and C_1, plus the voltage level of VCO_{in} at pin 9, provide direct control of the frequency. Resistors R_1 and R_2 fix the level of current bias to CMA1 and CMA2 for currents I_1 and I_2, respectively. Both CMA circuits consist of a current mirror with, typically, 6× to 8× gain. Because the frequency and offset-frequency amplifiers are source followers with 100% feedback, the voltage across R_1 at pin 11, V_{R1}, is equal to VCO_{in}, and the voltage across R_2 at pin 12, V_{R2}, is equal to V_{ref}. V_{ref} is an internal bias source set at one forward diode drop from V_{CC}. As such, the voltage across R_2 and the current I_2 are functions of V_{CC}, implying the need for a well-regulated V_{CC} for good offset-frequency stability. For most applications, $V_{ref} = V_{CC} – 0.6$ V is a good approximation. In the equations that follow, $I_1 = VCO_{in}/R_1$ and $I_2 = V_{ref}/R_2$ are used as direct expressions for the CMA input currents.

The outputs of CMA1 and CMA2 are the amplified M_1I_1, and M_2I_2 currents, where M_1 and M_2 are the multiplier ratios for CMA1 and CMA2, respectively. The CMA output currents then are summed together as the current, I_{sum}, to drive capacitor C_1 via the PMOS and NMOS transistors of G_1 and G_2. When the input to G_1 is high, the input to G_2 is low. In this mode, the PMOS transistor of G_1 conducts charge to C_1 while the NMOS transistor of G_2 discharges the low side of C_1 to ground. Each time the flip-flop changes state, the charging polarity of C_1 is reversed by G_1 and G_2. When the positively charged side of C_1 is grounded, an intrinsic diode across each of the NMOS devices discharges C_1 to one diode level below ground.

There are two C_1 charge cycles in each full period, and the instantaneous start voltage for each current-charged ramp is $V_{lr} = –0.7$ V. The active switch threshold at the flip-flop input is $V_{hr} = 1.1$ V for a V_{CC} of 5.0 V, and varies with V_{CC} (see Figures 16 and 17). Figure 17 shows the voltage waveforms at pins 6 and 7 as similar, except for the half-cycle displacement. The total peak-to-peak voltage of the sawtooth-ramp waveform at pins 6 or 7 is, typically, $V_{ramp} = [V_{hr} – V_{lr} = [1.1 – (–0.7)] = 1.8$ V.

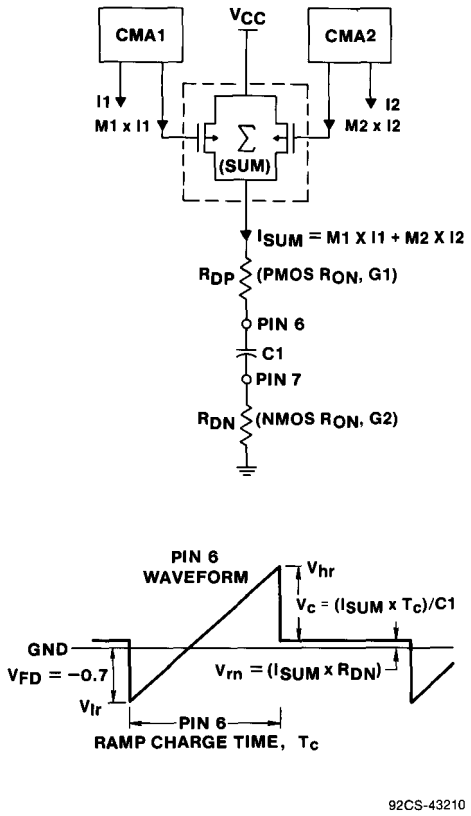


Figure 16. Equivalent HC/HCT4046A Charge Circuit of the VCO

VCO Frequency Control

When a capacitor, C, is charged with a constant current, I, the expression for the voltage, V_C, integrated over time, T_C, is:

$V_C = (1/C) \int Idt = (IT_C)/C$

In this case, the capacitor voltage is:

$$V_C = V_{ramp} = (V_{hr} - V_{lr}) = I_{sum}(T_C/C_1) \quad (1)$$

or

$T_C = C_1 \times V_{ramp}/I_{sum}$

Where:

$I_{sum} = [M_1 I_1 \times (M_2 I_2)]$

The time, T_C, is the ramp charge time, and V_{ramp} is the capacitor ramp charge voltage over the integrated time period. The ramp rate of voltage increase is V_{ramp}/T_C, and is determined by the rate of charge of the capacitor by the source current, I_{sum}.

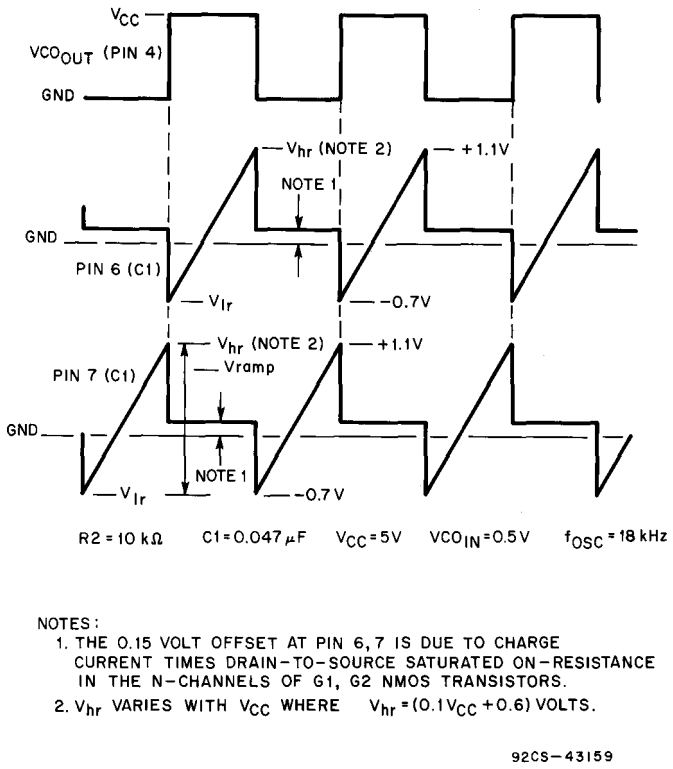


Figure 17. HC/HCT4046A VCO Waveforms

The CMA gain characteristics for M_1 and M_2 are shown in the curves of Figures 18–21. The values for M_2 as a function of I_2 are shown in Figure 18. The curves of Figure 19 show the CMA2 range of linearity for I_2 input. The linear range and values for multiplier M_1 are shown in the curves of Figures 20 and 21.

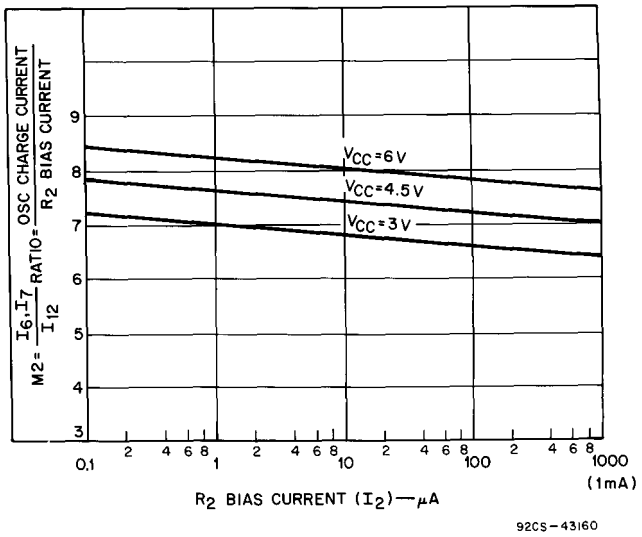


Figure 18. Current Multiplier Ratio M_2 as a Function of R_2 Bias Current

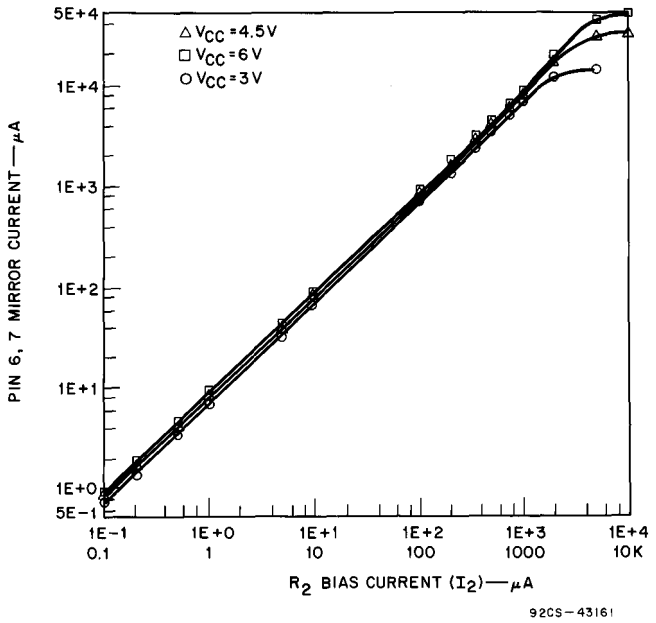


Figure 19. Mirror Current as a Function of R_2 Bias Current, Showing Range of Linearity

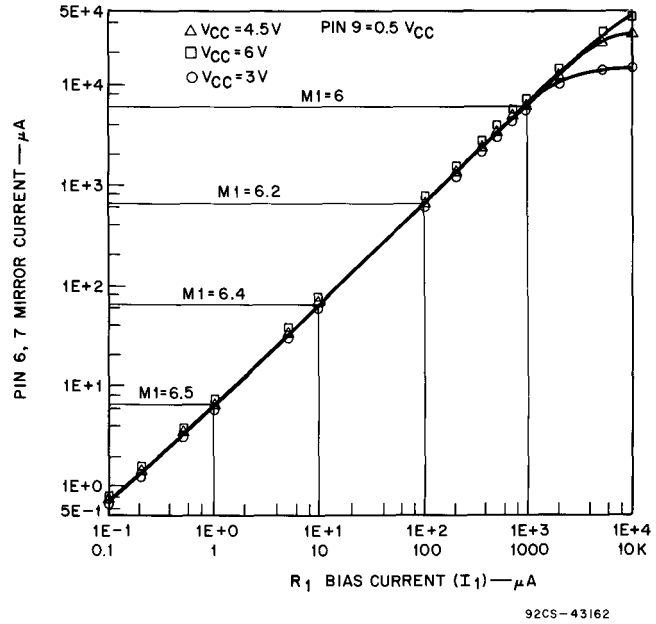


Figure 20. Mirror Current as a Function of R_1 Bias Current, Showing Range of Linearity (Pin 9 VCO_{in} = 0.5 V_{CC})

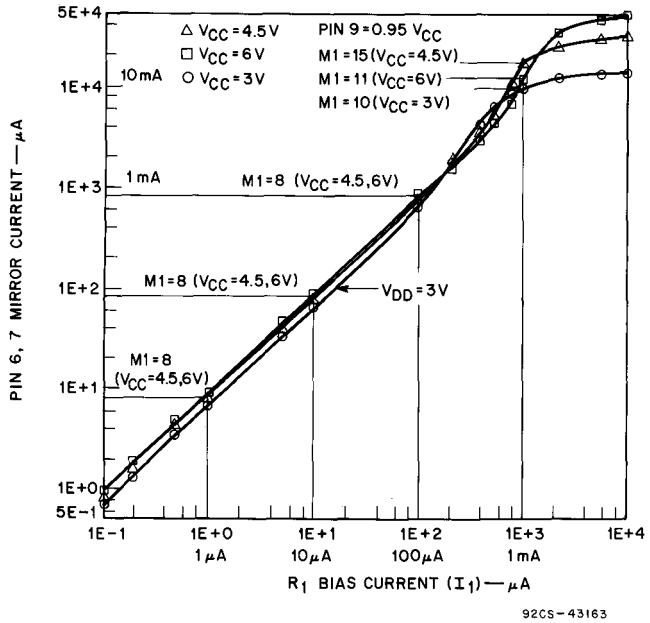


Figure 21. Mirror Current as a Function of R_1 Bias Current, Showing Range of Linearity (Pin 9 VCO_{in} = 0.95 V_{CC})

Equation 1 is sufficiently accurate to allow a good approximation of the VCO period ($2T_C$). However, there is a more precise equation for ramp charge time. In Figure 17, Note 1, attention is called to an offset voltage of approximately 0.15 V. Figure 16 shows the reason for this characteristic in an equivalent circuit, where the mode of switching is for the G_1 PMOS and G_2 NMOS transistors in their “on” charge state. The more precise form of the voltage equation should include the NMOS channel resistance, R_n.

Because the trip point, V_{hr}, is the sum of $V_c + V_{rn}$, and does not change in value, and $V_{lr} = V_c(0)$ is approximately –0.7 V as the initial charge condition on capacitor C_1:

$$V_{ramp} = V_{hr} - V_{lr} = (V_c + V_{rn}) - V_c(0) = I_{sum}T_c/C_1$$

Where:

$$I_{sum} = (M_1I_1) + (M_2I_2)$$

and, because $V_{rn} = I_{sum}R_n$:

$$T_C = (V_{ramp} - I_{sum}R_n)C_1/I_{sum} \quad (2)$$

Where:

V_{ramp} is the same as defined in Equation 1.

As noted previously, the initial voltage, $V_c(0)$ is one diode drop below ground, or –0.7 V, and is equal to V_{lr}. The V_{hr} trip point for the flip-flop does not change, and was noted to be, typically, 1.1 V for V_{CC} = 5 V. As shown in Figure 16, $V_{hr} = V_c + V_{rn}$. This expression shows that less charging time is needed to reach the trip point because V_c is reduced by the $I_{sum}R_n$ voltage drop. The $I_{sum}R_n$ term introduces a characteristic of nonlinear increasing frequency as a function of VCO_{in} voltage and is caused by the voltage drop in the NMOS channel resistance. When VCO_{in} is increased, the added M_1I_1 current continues to further reduce the sweep-time requirement. For large values of R_1 and R_2, the effect of resistance R_n is small, and the V_{rn} term in the above equations may be neglected.

When Equation 1 or 2 is used as a first-order approximation, a complete expression for frequency would incorporate timing for two ramps, plus the propagation delays for each flip-flop state, plus the added time for charging stray capacitance. Either case yields a ramp charge expression. The propagation delay, T_{pd}, is a function of the number of cascaded stages in the flip-flop, plus G_1 and G_2 switching propagation-delay times. The stray capacitance, C_s, from pin 6 to pin 7 (or from each pin to ground) must be added to the value of C_1. It should be noted that unbalanced capacitance to ground from pin 6 and pin 7 can contribute an unbalanced duty cycle. In fact, unbalanced capacitance at pin 6 and pin 7 may be used by design to correct or set the duty cycle. With the frequency-dependent parameters now defined, the VCO frequency becomes:

$$f_{osc} = 1/T_{osc} = 1/(2T_c + 2T_{pd}) \quad (3)$$

Using the simplified expression of Equation 1 to calculate the ramp charging time, and including the appropriate terms for capacitance $C_1 + C_s$, V_{ramp}, and I_{sum}:

$$T_c = [(C_1 + C_s) \times V_{ramp}]/[(M_1I_1) + (M_2I_2)]$$

which expands to :

$$T_c = [(C_1 + C_s)V_{ramp}]/[M_1(VCO_{in}/R_1) + M_2(V_{ref}/R_2)] \quad (4)$$

Where:

$$I_{sum} = [M_1(VCO_{in}/R_1) + M_2(V_{ref}/R_2)]$$

The more precise solution is:

$$T_c = [(C_1 + C_s)(V_{ramp} - I_{sum}R_n)]/I_{sum} \quad (5)$$

The value of T_c is calculated from Equation 4 or 5, and is substituted into Equation 3 to determine the frequency, f_{osc}. For the most part, Equations 3 and 4 provide a reasonably accurate and direct approach to determination of the frequency of the VCO in terms of external component values and known parametric voltage values.

VCO Parametric Ranges and Restrictions

When Equations 3 and 4 or 5 are used, it is necessary to adhere to certain range limitations for the components and to seek the correct parametric values for other variables. The following list tabulates the variables of the equations and defines ranges and restrictions.

V_{CC} — Defined in the HC/HCT4046A and HC/HCT7046A data sheets as 7 V maximum; for normal operation should remain in the range of 3 V to 6 V.

VCO_{in} — The pin-9 voltage, VCO_{in}, determines the frequency of the VCO. The control range is 1.0 V < VCO_{in} < 0.9 V_{CC}; the VCO becomes unstable if VCO_{in} exceeds the maximum. On the low side, the VCO is not responsive to input level until VCO_{in} is ≥ 1.0 V.

V_{ref} — The internal reference voltage, V_{ref}, is equal to one forward diode drop below V_{CC} (V_{CC} – 0.6 V). Where R_2 is used to fix offset frequency by current I_2, the V_{ref} level is maintained at pin I_2 (R_2) to set the source current, I_2.

V_{ramp} — Values for V_{ramp} are defined above with commentary on the effect of $I_{sum}R_n$ which, for many applications, is a second-order effect and can be neglected. As an empirically derived equation:
V_{hr} = (0.1 V_{CC} + 0.6) V and V_{ramp} = (V_{hr} – V_{lr}) = (0.1 V_{CC} + 1.3) V.

C_1 — The external VCO timing capacitor between pins 6 and 7 should be a larger value than 40 pF. Lower values are subject to device and layout tolerance variations caused by stray capacitance at pins 6 and 7.

C_s — Stray capacitance at pins 6 and 7 is not limited to pin-to-pin capacitance. Any stray capacitance at pin 6 or pin 7 must be charged and discharged during each normal oscillator cycle.

R_1 — The value of R_1 determines the frequency of the VCO for the defined $VC0_{in}$ range. The minimum (offset) frequency is determined by R_2, and that the current in R_1 is determined by $I_1 = VCO_{in}/R_1$.

R_2 — R_2 is frequently misused. The value of R_2 determines the offset (minimum) frequency of the oscillator. When there is no basic need for an offset frequency, R_2 should be omitted. If it is, no termination is needed at pin 12. When R_2 is not used and if the detector reference signal is removed, the oscillator's minimum frequency drops to zero. To sustain oscillation during signal dropout, some value of R_2 is needed. The current in R_2 is determined by $I_2 = V_{ref}/R_2 = (V_{CC} – 0.6)/R_2$.

M_1, M_2 — The currents I_1 in resistor R_1 and I_2 in resistor R_2 are multiplied in the current mirrors CMA1 and CMA2 and summed to provide the I_{sum} charging current to $C_1 + C_s$. The CMA multiplying factors are, respectively, M_1 and M_2. Figure 18 provides curve families for M_2 as a function of I_2 and V_{CC}. The nominal current-multiplier factor for M_1 is determined from the curves of Figure 20.

I_{sum} Where I_{sum} is defined as ($M_1I_1 + M_2I_2$), the total sum of $I_1 + I_2$ should not exceed 1.0 mA. The multiplier values of M_1 and M_2 typically are 6× to 8×. At higher levels of current, I_{sum} degrades VCO linearity. The limits of linear range in the curves of Figures 19–21 should be noted.

T_{pd} Inherent propagation delay as noted in Equation 3 is approximately 10 ns to 14 ns for the flip-flop in the feedback loop of the oscillator. For V_{CC} = 7 V, the propagation delay decreases approximately 10%. For V_{CC} = 3 V, the propagation delay increases approximately 30%.

T_c The ramp charge time, T_c, for capacitor C_1 is assumed to be equal for pin 6 to pin 7 or pin 7 to pin 6 in Equations 4 and 5.

f_{osc} The oscillator frequency for a given VCO_{in} as read at the VCO_{out}, pin 4. It may be calculated using Equations 3 and 4 or 5.

Design Examples With Measured And Calculated Results

Figure 22 shows measured data for the HC/HCT4046A for frequency, f_{osc}, as a function of VCO_{in} voltage. Using $R_1 = R_2 = 10$ kΩ, $C_1 = 47$ pF, $C_S = 6$ pF, and assuming $T_{pd} = 11$ ns in the circuit of Figure 23, curves for V_{CC} = 3 V, 4 V, 5 V, and 6 V were measured and plotted. The dashed lines for curves B, D, and E were calculated using Equations 3 and 4 and show that there is a reasonable agreement of measured and calculated results. The effect of an accelerated frequency increase is more noticeable in the V_{CC} = 5 V curve (curve E) with no offset (no R_2), where the measured frequency sweeps up with an increasing slope. The approximation equations, however, are still valid, varying from 5% to 15% error, mostly at the high VCO_{in} voltage values. The effects of no offset bias should be noted in the curve for V_{CC} = 5 V and R_2 = infinity (curve E). Without offset bias, all oscillation stops when the VCO_{in} voltage drops below 1.0 V.

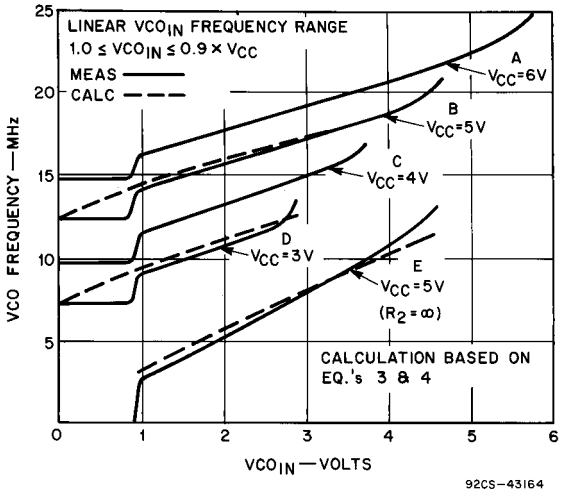


Figure 22. VCO Frequency as a Function of VCO_{in} (Measured and calculated values are shown. $R_1 = R_2 = 10$ kΩ, $C_1 = 47$ pF, $C_S = 6$ pF, $T_{pd} = 11$ ns at $V_{CC} = 5$ V, and $T_{pd} = 15$ ns at $V_{CC} = 3$ V)

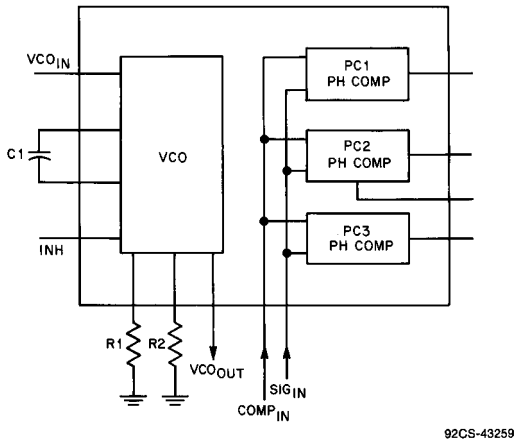


Figure 23. HC/HCT4046A PLL VCO Test Circuit

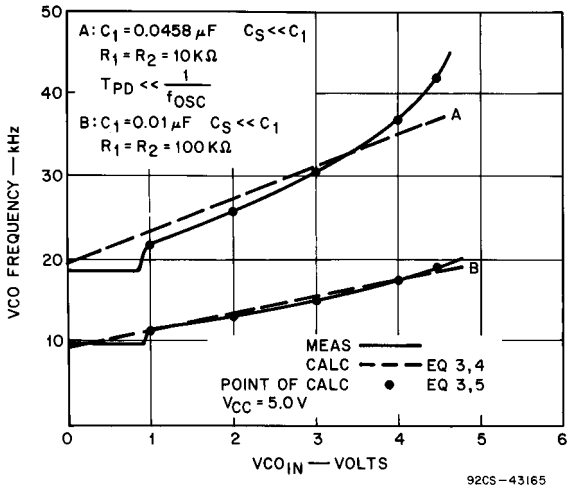


Figure 24. VCO Frequency as a Function of VCO_{in}, Showing Effects of Different Values of R_1 and R_2 (10 kΩ and 100 kΩ)

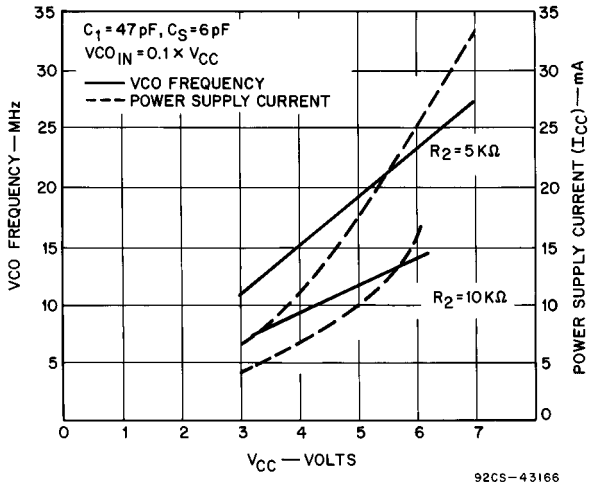


Figure 25. VCO Frequency and Power-Supply Current as a Function of Operating Voltage V_{CC}, Showing Effects of Different Values of R_2 (5 kΩ and 10 kΩ).

Although values of 10 kΩ for R_1 and R_2 provide good linearity as a function of VCO_{in} for the high-frequency range shown in Figure 22, optimum values for R_1 and R_2 are greater at lower frequencies. This fact is shown in Figure 24, where the linearity is better for the larger values of R_1 and R_2 (curve B). The accelerated frequency-increase effect of $I_{sum}R_n$ is more pronounced. The propagation delay is neglected in the curves of Figure 24 because it is much less than the oscillator period. The effects of stray capacitance are neglected for similar reasons. The simplified solutions using Equations 3 and 4 are shown by the dashed lines.

A more accurate calculation was made with Equations 3 and 5 to determine the value of I_{sum}. A value of 50 Ω was used to calculate the $I_{sum}R_n$ term. The calculated results for this curve quite accurately overlay the measured, solid-line curves. In this calculation, the values of M_1 and M_2 were set 15% low to obtain the exact tracking match.

Figure 25 shows measured data and illustrates the dependence of the offset frequency on V_{CC}. The frequency is in megahertz and the power-supply current in milliamperes. These parameters are plotted against power-supply voltage. I_{cc} is shown for R_2 offset-frequency bias resistors of 5 kΩ and 10 kΩ. The supply current increases with a decrease in the value of resistor R_2, and also increases with the switching frequency because of the added current needed to charge and discharge the device equivalent capacitance, C_{pd}.

Figure 26 shows the effect of increasing the values of resistors R_1 and R_2 by 10× with all other factors remaining the same. Curve A is plotted at 10× the measured frequency, while curve B is plotted at the frequency of the measured data. The two curves should overlay one another. The current multiplier ratios, however, are higher at lower current bias levels, a factor that causes the frequency defined by curve A to be slightly more than 10× that of curve B. The curves illustrate that frequency can be changed by a linear scale factor with a change in R_1 or R_2. Similar frequency changes also can be made by adjusting C_1. An exception is that effects of T_{pd} and C_s produce a ratio-adjustment error in the high-frequency range. Figure 27 demonstrates the results of a different method of frequency control by "splitting" capacitor C_1 and returning pin 6 and pin 7 separately through capacitors C_{1A} and C_{1B} to ground. Illustrated in Figure 28, this method can control the duty cycle, which is the ratio of capacitors C_{1A} and C_{1B}. The V_{ramp} conditions change from –0.7 V as a starting point to ground or 0 V. The V_{hr} trip point is unchanged. The current charge path for each capacitor is through its respective G_1 or G_2 PMOS device, and the discharge path is through the associated NMOS device. Frequency calculations for this type of circuit are based on a separate calculation for each capacitor charge ramp and the addition of the results for the total period time. The same equations are used in the calculations, but the empirical equation for V_{ramp} becomes:

$$V_{ramp} = V_{hr} - V_{lr} = 1.1 - 0 = 1.1 \text{ V}$$

Where:

$$V_{CC} = 5.0 \text{ V}$$

For other V_{CC} values, $V_{hr} = (0.1\ V_{CC} + 0.6)$ V. The simplified calculation is shown by the dashed line in Figure 27 to be in reasonable agreement with empirical results. Where the RC discharge might not reach ground before the charge cycle starts, $V_{lr} = V_c(0)$ assumes this value. The waveform characteristic is shown in Figure 28.

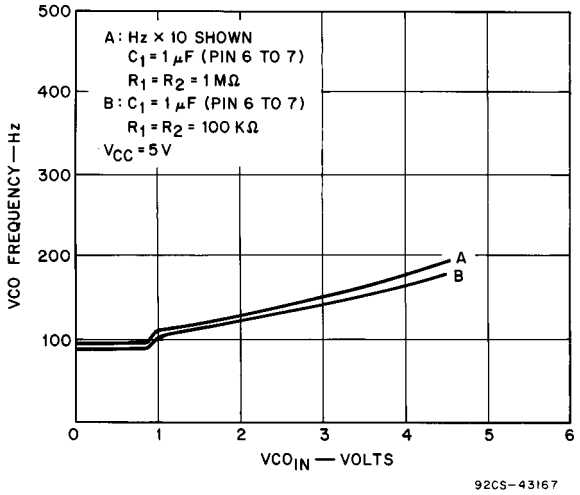


Figure 26. VCO Frequency as a Function of VCO_{in}, Showing Effects of Different Values of R_1 and R_2 (10 kΩ and 1 MΩ)

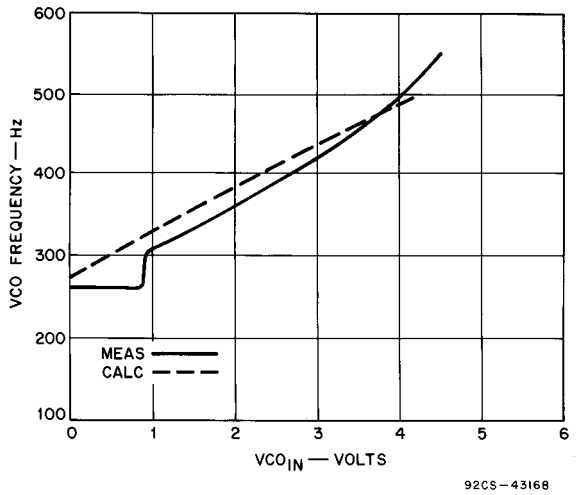


Figure 27. VCO Frequency as a Function of VCO_{in}, Showing Duty-Cycle Control Obtained by Splitting Capacitor C_1 and Controlling the Ratio of C_{1A} and C_{1B}

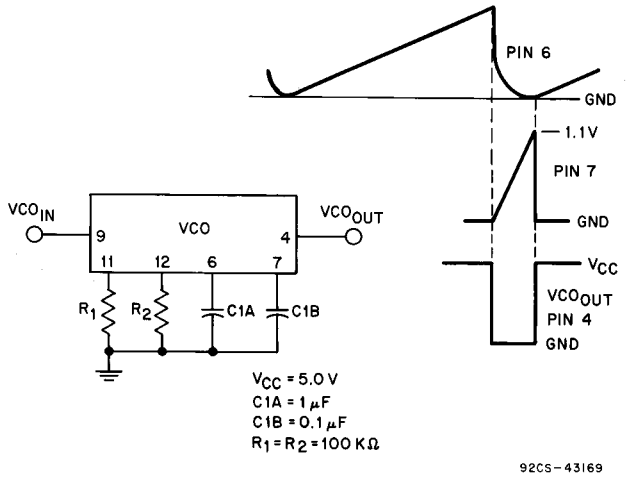


Figure 28. Evaluation Circuit and Waveforms for Data in Figure 27

Possible applications of the split-capacitor method described in previous paragraphs include horizontal and vertical timing circuits for image-display systems, as well as gating and blanking functions where, for a variety of reasons, pulse-duration control is needed.

Design Examples With and Without Offset

The equations derived thus far have provided a means to calculate frequency. However, frequency usually is the known parameter. If it is not known, an approximation initially can be calculated, followed by an iterative adjustment for the final desired result. Dynamic-range limitation can be accommodated more easily by following this procedure.

Example With Offset

For a supply voltage V_{CC} = 5 V and given:

f_o (center frequency) = 400 kHz
f_{min} (offset frequency) = 250 kHz
$f_{max} = f_{min} + 2(f_o - f_{min})$ = 550 kHz

The curves plotted thus far indicate that a value of 0.01 μF can be a suitable value for C_1, and that propagation delay and stray capacitance can be neglected. For convenience, assume that the multiplying factor $M = M_1 = M_2 = 7.2$ and, from previously noted values, V_{ramp} = 1.8 V. First, calculate the offset frequency by setting VCO_{in} = 0 V. With these simplified conditions, Equations 3 and 4 become:

$$f_{min} = 1/2T_c = 1/2\ (C_1V_{ramp}/M_2I_2)$$
or
$$f_{min} = 2M_2V_{ref}/C_1V_{ramp}R_2$$

Where:

$$I_2 = V_{ref}/R_2 = (V_{CC} - 0.6)/R_2 = 4.4/R_2$$

Solving for R_2 yields:

$$R_2 = M_2V_{ref}/2C_1V_{ramp}f_{min}$$
$$= (7.2 \times 4.4)/(2 \times 0.01\ \mu F \times 1.8 \times 250\ kHz)$$
$$= 3.52\ k\Omega$$

If this low value of R_2 is used, the resultant $I_{sum}R_n$ causes pronounced nonlinearity, as shown in Figure 24, curve A. Better linearity can be achieved with an R_2 of 35.2 kΩ and by scaling frequency; C_1 also can be set to 1000 pF. This choice seems practical because the assumption is that stray capacitance, C_S = 6 pF, which is not a significant percentage of C_1. R_2 should be further adjusted by choosing a value for it of 36 kΩ, which is close to a standard value of resistance.

From the known maximum frequency, f_{max}, and given the value of R_2, R_1 can be calculated. Assume that the maximum frequency occurs at approximately $VCO_{in} = V_{ref}$ = 4.4 V. The same values of M_1 and M_2 as used above will continue to be used for this approximation. The problem now is to find a parallel value of R_1 and R_2 (R_{eq}) for the calculation of f_{max}:

Where:

$$R_{eq} = MVCO_{in}/2C_1\ V_{ramp}f_{max}$$
$$= (7.2 \times 4.4)/(2 \times 1000\ pF \times 1.8 \times 550\ kHz)$$
$$= 16\ k\Omega$$

For R_2 = 35.2 kΩ, R_1 is determined to be 29.3 kΩ, or approximately 30 kΩ to the nearest standard value. With these values and Equations 3 and 4, the calculations for the frequency can be fine tuned. With V_{ref}/R_2 at 122 μA, M_2 from Figure 18 becomes 7.3. Similarly, when $VCO_{in} = V_{CC}/2$, VCO_{in}/R_1 = 83 μA, which, from Figure 20, yields M_1 = 6.2.

T_c and f_{osc}, as a function of VCO_{in}, can be calculated from these values and, if needed, R_1 and R_2 can be adjusted to meet the desired center-frequency condition. That is, for $C_s = 0$, $T_{pd} = 0$, $R_1 = 30\ k\Omega$, $R_2 = 36\ k\Omega$, $C_1 = 1000$ pF, $V_{ref} = 4.4$ V, $V_{ramp} = 1.8$ V, $M_1 = 6.2$, $M_2 = 7.3$, and $V_{CC} = 5$ V:

$$f_{osc} = 1/2T_c = [M_1(VCO_{in}/R_1) + M_2(4.4/R_2)]/2C_1V_{ramp}$$
$$= [6.2(VCO_{in}/30\ k\Omega) + 7.3(4.4/36\ k\Omega)]/(2 \times 1000\ pF \times 1.8\ V)$$

Calculated and measured oscillator frequency values for different values Of VCO_{in} are:

VCO_{in} (V)	f_{osc} (kHz)	
	CALCULATED	MEASURED
0.0	248	280
1.0	305	318
2.5	391	384
4.4	500	492

The calculated solution is in reasonable agreement with the desired results, as shown by the measured data. Depending on the application, some adjustment of R_2 might more closely fit the f_{osc} value.

Example Without Offset

Given: $f_o = 400$ kHz, $V_{CC} = 5.0$ V

Without offset, the calculation is simplified to:

$$f_{osc} = 1/2T_c = M_1(VCO_{in}/R_1)/2C_1V_{ramp}$$

Drawing on the experience of the previous calculation, M_1 is approximately 6.2 and VCO_{in} is set to 2.5 V for the center-frequency calculation. Solving for R_1:

$$R_1 = 6.2\ (2.5/f_o)/(2 \times 1000\ pF \times 1.8\ V) = 10.8\ k\Omega$$

Using 11 kΩ for R_1, gives:

VCO_{in} (V)	f_{osc} (kHz)	
	CALCULATED	MEASURED
1.0	157	139
2.5	391	352
4.4	699	697

In this example, the error is larger, but the dynamic range needed for the high and low ends of the frequency range is there. The center-frequency value of VCO_{in} is slightly to the high side of 2.5 V.

Rules of Thumb for Quick Calculations

The previous examples imply that simple equations and rules of thumb can be effectively applied to the determination of required parameters. Designers, however, should remain alert to the fact that large values of I_{sum} with frequencies in the megahertz range do require use of the expanded Equations 3, 4, and 5. For extreme ranges of current and voltage, other errors may be added. However, reasonable approximations of the offset frequency, f_{min}, and the maximum frequency, f_{max}, can be made. Where $T_{pd} << 1/f_o$ or the frequency range is less than 1.0 MHz and the I_{sum} currents are reduced so that $I_{sum}R_n << V_{ramp}$, the errors generally will be less than 15%. The quick-approximation equations are derived as follows:

From Equation 4, solving for $f_{min} = 1/2T_c$ at V_{CC} = 5 V, VCO_{in} = 0 V, C_s = 0 pF, V_{ramp} = 1.8 V, and $M_1 = M_2 = 7$ yields:

$$f_{min} = K_a/(R_2C_1) \quad (6a)$$

Where:

K_a is a constant that varies with V_{CC}.

where K_a is a constant that varies with V_{CC}.

To find f_{max} with $VCO_{in} = V_{ref}$ = 4.4 V, V_{CC} = 5 V, C_s = 0 pF, V_{ramp} = 1.8 V, and $M_1 = M_2 = 7$,

$$f_{max} = K_a/(R_{eq}C_1) \quad (6b)$$

Where:

R_1 in parallel with $R_2 = R_{eq}$.

Then, an extrapolation from f_{min} at VCO_{in} = 0 to f_{max} at VCO_{in} = 4.4 V yields a quick y = mx + b equation approximation to f_{osc}:

$$f_{osc} = [(f_{max} - f_{min})/K_b]VCO_{in} + f_{min} \quad (6c)$$

Where:

K_b at f_{max} is 4.4 for V_{CC} = 5 V, or 5.4 for V_{CC} = 6 V.
K_a at f_{max} and f_{min} is 8.5 for V_{CC} = 5 V and 10 for V_{CC} = 6 V.

The solution is provided as a time constant for R_2C_1 or $R_{eq}C_1$, where C_1 is assumed, followed by a calculation for R_1 and R_2.

The choice of offset frequency is not as simple as it first appears. The true offset with respect to phase lock starts when the VCO_{in} is approximately 1.0 V. The lock-in range where $2f_I = (f_{max} - f_{min})$ is limited by this condition. As such, the lock-in range is only 60% of the VCO_{in} control range for VCO_{in} = 0 V to VCO_{in} = 2.5 V or (V_{CC}/2). Using the lower VCO control range as a boundary condition for lock-in, $0.6(f_o - f_{min}) = f_I$.

Where f_{min} is the offset frequency, the rule-of-thumb equation for offset in terms of center frequency and lock range is:

$$f_{min} = f_o - 1.6f_I \quad (6d)$$

Tabulated Solutions

The expanded Equations 1 through 5 have been written into a computer program using empirically derived equations from the curves and data for I_1, I_2, M_1, M_2, and T_{pd}. This program is included in Appendix C. PC calculations and rule-of-thumb solutions have been calculated and compared to measured data to evaluate the frequency error in several applications. Appendix IV gives R_1, R_2, and C_1 values with "Calc. f_{osc}" PC solutions from Equations 3, 4, and 5. The "Approx. f_{osc}" values are given by the rule-of-thumb solutions from Equations 6(a), 6(b), and 6(c).The solutions shown below are based on high and low inputs to VCO_{in}, and have larger estimate errors than those previously shown and plotted. The most accurate frequency calculations are determined by having the correct values for M_1 and M_2, which, for the full range of VCO_{in}, are not constant. The preferred solutions are derived for a VCO_{in} voltage near $V_{CC}/2$, where the curves for I_1 as a function of pin 6 and pin 7 current plots are most accurate. The example data given here is based on single result values from constructed PC boards (see Appendix V).

Filter Design for the HC/HCT4046A

The third element of the HC/HCT4046A PLL to be discussed is the filter requirements for proper operation of the loop. An understanding of various technical terms is assumed. For further assistance, the reader is referred to Appendix B and the bibliography. It is important to remember that the filter characteristic is a key factor in determining the overall gain and phase response of the loop. Stability criteria are covered in general references on feedback theory along with other subjects, including Bode plots, root-locus plots, and Nyquist criteria. The use of Laplace transforms with partial fraction expansions, the final-value theorem, and other techniques should be very helpful to the dedicated designer of PLL circuits. Loop equations in Figure 29 are expressed in terms of the complex-frequency domain.

Three basic types of LPFs are commonly used in PLL circuits. All LPFs perform the basic function of removing high-frequency components resulting from the multiplier process of the phase comparator. Figure 29 shows these common forms of the LPF along with equations for the loop as applied to PLLs of second-order systems.

Another characteristic of the PLL is phase jitter, which may occur because the VCO is frequency modulated by the ripple output of the LPF. Moreover, noise may initiate fast changes in phase error and cause conditions of variable damped oscillation in the loop. Characteristics common to the PLL are noted in the following discussion, which also provides examples and data.

The LPF integration properly determines the time constant of the filter and affects the loop during frequency acquisition. A low-leakage termination for the filter provides a constant dc level to the VCO and maintains a minimum phase-shift relation between the VCO signal and the PLL input signal. The HC/HCT4046A features a very high resistance load to the LPF where the input resistance of the VCO is of the order of 10^{12} Ω. In many applications, particularly at high frequency, leakage currents can cause an unacceptable phase error.

Loops are frequently referred to by type and order designation. Type is less commonly used and refers to the number of perfect integrators in the loop or the number of poles at the origin of the complex-frequency plot. An example of a Type I would be a simple first-order PLL where there is no filter [f(s) = 1]; integration of the VCO provides the one pole. The order of the loop is a more commonly used term and refers to the highest power of s in the denominator of the closed-loop transfer function, H(s). The application examples that follow are based on second-order systems, which represent the most common use of PLL circuits employing the HC/HCT4046A.

Loop Examples

LPF Using PC1 (Example 1)

This first example shows the effects of parameter variation; PC1 and the simple RC-lag LPF of Figure 29 are used. The conditions for this example are:

f_o = 27.5 kHz and f_{min} = ? kHz
V_{CC} = 6 V, VCO_{in} range is 1 to 5.5 V

The tendency for the novice designer is to specify an offset frequency close to the desired center frequency. This choice reduces the VCO gain factor and adds a resistor to the circuit. The need for an offset frequency specification always should be questioned. Occasionally, an offset frequency may be needed if the application requires continuing oscillation when the VCO_{in} input drops below 1.0 V. The arbitrary assumption in this example is the choice of f_{min} = 0 or no offset.

To find the VCO parameters, the designer should initially calculate R_1 and C_1 by considering the VCO_{in} level at $V_{CC}/2$ or 3 V. For this working frequency range, the consideration of stray capacitance and propagation delay can be dropped. Using the rule-of-thumb equation developed in the VCO section, the y = mx + b equation form can be used for f_{min} = 0 and V_{CC} = 6 V, where K_a = 10 and K_b = 5.4. Then, R_{eq} reduces to R_1 and Equations 6(b) and 6(c) combine as:

$$f_{osc} = VCO_{in}/(0.54R_1C_1)$$

By choosing C_1 = 0.012 µF, R_1 becomes 16.8 kΩ for VCO_{in} = 3 V and $f_{osc} = f_o$ = 27.55 kHz. The actual component values used were R_1 = 16.4 kΩ and C_1 = 0.012 µF. Frequency calculations for a VCO_{in} of 1 V and 3 V using the above equation are:

VCO_{in} (V)	f_{osc} (kHz)	
	CALCULATED	MEASURED
1.0	9.4	–
1.24	11.7	10
3.0	28.2	–
3.34	31.4	27.5

The values shown are a reasonable approximation of the required values.

The VCO gain factor, K_o, must be determined for the filter design. Either the slope of the curve for f_{osc} as a function of VCO_{in} can be used, or a value can be calculated from the differentiated frequency expression. If $I_{sum}R_n << V_{ramp}$, the $I_{sum}R_n$ term may be dropped. In this case, the calculated error is approximately 3% at $VCO_{in} = V_{CC}/2$. Using Equations 3 and 4, substituting T_c into the f_{osc} equation and dropping the $I_{sum}R_n$ and T_{pd} terms yields:

$$f_{osc} = I_{sum}/2C_1V_{ramp} = M_1VCO_{in}/2R_1C_1V_{ramp}$$

The differential with respect to VCO_{in} is given by:

$$K_o = d(f_{osc})/d(VCO_{in}) = M_1/2R_1C_1V_{ramp}$$

This result is the same as the differential of $VCO_{in}/(0.54R_1C_1)$ if $M_1 = 7$ and $V_{ramp} = 1.9$ V are assumed.

Substituting values $M_1 = 7$, $V_{ramp} = 1.9$ V, $R_1 = 16.4$ kΩ, and C = 0.012 pF yields:

$$K_o = 9.4 \text{ kHz/V or } 59.1 \text{ krad/V}$$

The K_d gain factor for the PC1 detector can be calculated as:

$$K_d = V_{CC}/\pi = 6/3.1416 = 1.91 \text{ V/rad}$$

The loop-gain factor, not including the filter, is given by:

$$K = K_oK_d = 112{,}800$$

As shown in Figure 29, for any second-order system, the loop natural frequency, ω_n, is:

$$\omega_n = (K/\tau)^{0.5}$$

Where:

τ is the integrating time constant of the loop filter.

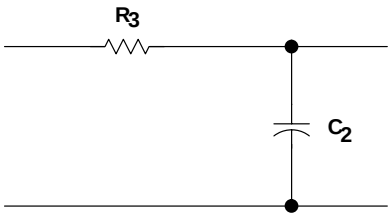
For the simple lag filter of Figure 29(a), $\tau = R_3C_2$.

Beyond this point, assumptions or specifications are needed, with respect to the design requirements. One may optimize for noise, jitter, sweep rate, pull-in time, etc., depending on the application. For general and wide-ranging requirements, values for the loop 3-dB bandwidth, ω_{3dB}, and loop natural frequency can be assumed. Another choice is to look at the relation of noise bandwidth to damping factor, ζ. If settling time is important, examine the phase error and damping factor as a function of $\omega_n t$ (t = time) where, for the settling time to be 90% complete, the value of ω_n, is given by the allowed settling time. Quoting from Gardner[1], and others, for a phase error due to a step in deIta phase, $\omega_n t$ should be 4 for a damping factor of 0.5.

The simple lag filter has a limited range of capability, but it can be effective in noncritical applications. The R_3C_2 time constant can be chosen by trial and error or by rule of thumb as the reciprocal of 1.5 to 3 times the frequency. This approach favors lower damping factors to achieve low jitter with compromises for pull-in range and time. Two filters were tried for this example:

τ_1	R_3	C_2	PULL IN	ω_n (CALCULATED)	ζ (CALCULATED)
2.5 ms	51 kΩ	0.047 µF	±1kHz	6717 rad/s	0.032
25 µs	51 kΩ	487 pF	±4.25 kHz	67.17 krad/s	0.32

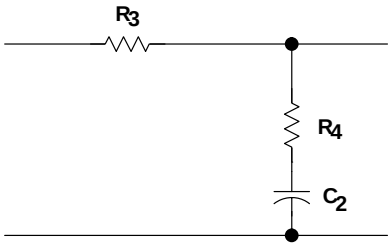
When filters are designed by choosing a ω_{3dB}/ω_n ratio, the simple lag filter has a solution in terms of ζ that is different from that of the lag-lead solution. In any case, the ω_{3dB} solutions are derived by setting $|H(j\omega)|^2 = 0.5$ and solving for ω_{3dB}/ω_n. However, experience is the best teacher, and the assumption of time-constant values, followed by the measuring and plotting of results, is an effective way to optimize values for those parameters important to an application.



(a)

$F_1(s) = 1/(s\tau_1 + 1)$
$\tau_1 = R_3C_2$
$H_1(s) = [\omega_n^2/(s^2 + 2\zeta\omega_n + \omega_n^2)]$
$\omega_n = (K_oK_d/\tau_1)^{0.5}$
$\zeta = (1/4\tau_1K_oK_d)^{0.5}$

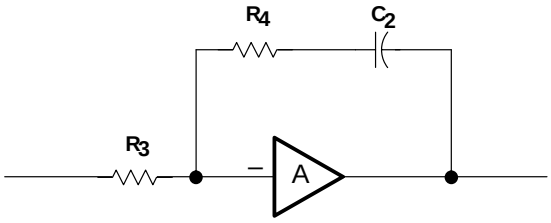
92CS-43170



(b)

$F_2(s) = (s\tau_2 + 1)/[s(\tau_1 + \tau_2) + 1)$
$\tau_1 = R_3C_2$
$\tau_2 = R_4C_2$
$H_2(s) = [s(2\zeta\omega_n - \omega_n^2) + \omega_n]/(s^2 + 2\zeta\omega_n + \omega_n^2)$
$\omega_n = [K_oK_d/(\tau_1 + \tau_2)]^{0.5}$
$\zeta = (\omega_n/2)[\tau_2 + (1/K_oK_d)]$

92CS-43171



(c)

For large values of A (amplifer gain):

$F_3(s) = -(s\tau_2 + 1)/s\tau_1$
$\tau_1 = R_3C_2\tau_2 = R_4C_2$
$H_3(s) = (2\zeta\omega_n s + \omega_n^2)/(s^2 + 2\zeta\omega_n s + \omega_n^2)$
$\omega_n = [K_oK_d/\tau_1)^{0.5}$
$\zeta = \omega_n\tau_2/2$

92CS-43172

Figure 29. Forms of LPF and Associated Loop Equations

Using PC2 With a Lag-Lead Filter (Example 2)

In this example, the lag-lead filter shown in Figure 29(b) is used, and no offset-frequency requirement is specified. For the VCO section:

V_{CC} = 6 V, f_{osc} = 1.2 MHz at VCO_{in} = 4.5 V

After following procedures similar to those described in Example 1, the value of C_1 is determined to be 100 pF, and R_1 is found to be 62 kΩ. The VCO measurements are:

f_{osc} = 1.16 MHz at VCO_{in} = 4.5 V

f_{osc} = 380 kHz at VCO_{in} = 1.6 V

and the following can be calculated:

$K_d = V_{CC}/4\pi$ = 0.48 V/rad
K_o = (1.2 – 0.38) MHz × 2π/(4.5 – 1.16)V = 1.77^6 rad/V
$K = K_oK_d = 0.85^6$

The relation of the filter bandwidth, defined as ω_f, can be used to establish the relation of τ_1 and τ_2 in the lag-lead filter. Then, defining the ratio of ω_f to ω_n provides a practical basis for comparing time constants to the active parameters of the loop. The solution of $|f(j\omega)|^2 = 0.5$ yields:

$$\omega_f = \frac{1}{\left(\tau_1^2 + 2\tau_1\tau_2 - \tau_2^2\right)^{0.5}}$$

which may be used to calculate τ_1 and τ_2 after the ω_f/ω_n ratio is assumed. Then, using the equation of Figure 29(b):

$\omega_n = [K/(\tau_1 + \tau_2)]^{1/2}$

filter-component values R_3, R_4, and C_2 can be derived as follows:

Given: ω_f = 1% of f_{min}, ω_f/ω_n = 1/8

Calculate: τ_1 = 0.0346 ms, τ_2 = 0.0092 ms
R_1 = 51 kΩ, R_4 = 1.36 kΩ
C_2 = 0.00068 μF

Where jitter is the ratio of phase displacement to signal period, the following PLL results were obtained:

SIG_{in} (kHz)	JITTER (ns)	PERCENT OF PERIOD
1200	<28	2.4
790	<20	1.6
380	50	1.9

Simple LPF Using PC2 (Example 3)

This example uses the results of Example 1 and redefines the criteria for the loop:

Given: ω_f = 100 Hz, ω_f/ω_n = 1/10
K_d is now $V_{CC}/2\pi = 6/2\pi$ = 0.955 V/rad

Basing this example on measured data:

K_o = 51400 rad/V
$K = K_o \times K_d$ = 49095

Using $\omega_n = (K/\tau_1)^{0.5}$ and the value of ω_n, from the given data gives:

τ_1 = 1.24 ms, R_3 = 51 kΩ, C_2 = 0.024 μF

Measured results give 0.5 μs of jitter (1.4% of period) at 27.5 kHz.

Simple LPF Using PC2 With Divide-by-N (Example 4)

This example uses one of the examples given previously in the VCO measured-data section:

V_{CC} = 6 V
R_1 = 43 kΩ, C_1 = 39 pF
For K_o, f_{osc} measured at VCO_{in} = 3 V
$K_o = 6.12^6$ rad/V
K_d = 0.955 V/rad (from previous example)

Using the HC4024 seven-stage binary ripple counter for a divide-by-N of 128 and PC2 in a simple RC LPF, the loop frequency is 20 kHz and

$K = K_o(K_d/N)$ = 45660

If it is assumed that ω_f is 1% of the loop frequency or ω_f = 200 Hz, and that ω_f/ω_n = (1/8), $\omega_n = (K/\tau_1)^{0.5}$ gives a time constant, τ_1, of 451 ms. Choosing R_3 = 51 kΩ gives C_2 = 0.0088 μF. The jitter measured during lock was less than 0.6 μs or 1.2%.

A tabulation of results using the same VCO and divide-by-N ratio, where ω_f is 1% of the 20-kHz loop (200 Hz) and ω_f/ω_n is varied, is shown in Table 1.

Table 1. Results for Simple LPF Using PC2 With Divide-by-N

ω_f/ω_n	ω_n (CALCULATED) (rad/s)	τ_1 (CALCULATED) (ms)	R_3 (CALCULATED) (kΩ)	C2 (CALCULATED) (μF)	JITTER (MEASURED) (μs)	ζ (CALCULATED) (d.f.†)
3	3774	3.206	51	0.0628	5	0.041
5	6290	1.154	51	0.0226	2	0.069
8	10064	0.451	51	0.0088	0.6	0.11
10	12580	0.288	5	0.0056	1.2	0.14

† d.f. = damping factor

The range of pull-in remained typically the same for the 20-kHz loop. The pull-in measured 6 kHz to 37 kHz.

Simple RC LPF Using Frequency Offset and PC2 (Example 5)

To provide a comparison with loop Example 4, a VCO example without the divide-by-N was developed using R_1 = 160 kΩ, R_2 = 180 kΩ, and C_1 = 0.005 μF. The measured frequency for V_{CC} = 6 V is:

$K_o = 2\pi(22780 – 20000)/(3 – 1.75) = 13973$ rad/V
$K_d = 0.955$ V/rad
$K = K_oK_d = 13344$

Using ω_f = 200 Hz and ω_f/ω_n = 1/10, and solving as above gives the results in Table 2.

Table 2. Results for Simple RC LPF Using Frequency Offset and PC2

ω_f/ω_n	ω_n (CALCULATED) (rad/s)	τ_1 (CALCULATED) (ms)	R_3 (CALCULATED) (kΩ)	C2 (CALCULATED) (μF)	JITTER (MEASURED) (μs)	ζ (CALCULATED) (d.f.†)
3	3774	3.206	51	0.011	5.5	0.18
6.3	7952	1.154	51	0.0041	4	0.3
8	10064	0.451	51	0.00161	2	0.48
10	12580	0.288	51	0.001	0.6	0.6

† d.f. = damping factor

The pull-in typically is 18 kHz to 33 kHz for this example. It should be noted that the damping factor, ζ, is higher than in Example 4. With offset, the loop-gain factor, K, is approximately one-third less.

VCO_{in} (V)	f_{osc} (MEASURED) (kHz)
0	15.38 (offset)
1	17.85
1.75	20
3	22.78

LPF Design Summary

There are several points to be made on the subject of LPF design. The examples shown in this application report are given as illustrations of HC/HCT4046A PLL capability. Indeed, the best recommendation for a general-purpose PLL would be to use an active filter. The gain factor, K, then would provide another degree of latitude in the many compromises of PLL design. The second-best filter would be the lag-lead filter network design, where the added resistor provides a semi-independent control over the damping factor of the loop, a key requirement in tracking systems. The lag-lead, however, is an imitation of the active filter only for a limited range of component values. If the primary requirement is to phase lock two frequencies synchronously together and response time is not a major factor, the simple RC filter may be quite adequate for this purpose.

Because the filter design is not rigid, options exist to vary the design approach. Optimizing by trial and error should be considered in all cases. One should always be aware that textbook approaches often are developed for applications not identified or with limitations and assumptions not given. A few points that may help to clarify the assumptions made in the examples given in this application report are:

- Open-loop analysis has limited significance. The PLL is a system within itself, and nearly all technical material is presented in the form of a closed-loop analysis. The bottom line is that the filter must be designed with the entire loop in mind.
- The HC/HCT4046A VCO gain factor, K_o, is dependent on the center frequency, f_o, and the offset frequency, f_{min}. That is, K_o is approximately $(f_o - f_{min})/(V_{CC}/2)$. If any of the VCO parameters such as R_1, R_2, or C_1 change, K_o and the filter design requirements will change.
- The use of a filter bandwidth of 1% of the signal or loop frequency may not achieve the desired results in all applications. Because no specific applications were defined in the preceding paragraphs, the 1% filter bandwidth, ω_f, was chosen as a practical way to achieve simple phase-lock results, given that ω_f/ω_n is chosen for a practical range of component values. In any case, the designer should be aware of the common parameters used to describe the PLL performance, such as damping factor (ζ) loop natural frequency (ω_n), noise bandwidth (BL or 2BL), and the loop gain ($K = K_oK_d$).
- The damping factor can be used as a starting point for design assumptions. For some applications, this approach could be a better one than choosing bandwidths. The system response, however, must take into account both the loop natural frequency and the damping factor.
- As noted in the VCO description, the linear range of the HC/HCT4046A extends from 1 V to approximately V_{CC} – 1 V. Operation of the VCO_{in} at or near the V_{CC} level is not recommended because the linear range of the internal differential amplifiers (CMA circuit) is exceeded. When this level of operation occurs, the K_o of the VCO increases rapidly and may cause loop instability. The application of active operational-amplifier filter circuits, using such devices as the CA5470, can limit the maximum positive voltage swing to approximately the correct level while operating from the same V_{CC} supply as the HC/HCT4046A.

The designer should apply high-speed application-circuit techniques when using high-speed CMOS PLL devices; the switching speed can produce higher-harmonic components. Good radio-frequency bypassing techniques with good filtering are recommended in the design of the power-supply distribution to minimize potential EMI problems.

Bibliography and References

1. *Phase-Lock Techniques*, F. M. Gardner, John Wiley & Sons, NY.
2. *Frequency Synthesis*, V. F. Krupa, John Wiley & Sons, NY.
3. *Engineering Electronics*, J. D. Ryder, McGraw Hill, NY.
4. “Color-Carrier Reference Phase Synchronization Accuracy in NTSC Color Television,” D. Richman, *Proceedings IRE*, 42:106–133, 1954.
5. “Miniaturized RC Filter Using Phase-Locked Loop”, G. S. Moschytz, *Bell System Tech. Journal*, p. 829, 1965.

Acknowledgments

Contributions to this application report were provided by J. Nadolski (device characteristics) and C. Lee (PLL filter examples).

This application report, which was acquired from Harris Semiconductor, who acquired it from RCA, has been edited and reformatted by Texas Instruments.

Appendix A Phase-Comparator Summary Information

TYPE	PC1 XOR	PC2 POSITIVE-EDGE-TRIGGERED J-K FLIP-FLOP	PC3 POSITIVE-EDGE-TRIGGERED R-S FLIP-FLOP
PC_{out} V_{PC} (out), (SIG_{in} high)	$V_{DD}/2$	Low	High
Locked phase differential, ϕ (SIG_{in} reference)	$\pi/2$	0	π
Filtered PC_{out}, V_{DEMout}	$V_{CC}/\pi) \phi$	$(V_{CC}/4\pi) \phi$	$(V_{CC}/2\pi) \phi$
Requires 50% duty cycle?	Yes	No	No
Lock detector	No	Yes (HC/HCT7046A)	No
Phase pulses out	No	Yes (HC/HCT4046A)	No

Appendix B Loop Parameters and Equations

Figure 1 shows the fundamental PLL block diagram and the relationships of the various loop parameters. The relationships of these parameters are determined by the transfer characteristic of each functional block of the loop. Brief explanations of parameter functions are provided in the following paragraphs. Further details can be found in various reference texts.

K_d Phase-comparator conversion gain factor expressed in units of V/rad. K_d is determined by the equation $V_d = K_d(\phi_i - \phi_o)$ or $K_d = V_d/(\phi_i - \phi_o)$. For the phase comparators of the HC/HCT4046A, $V_d = V_{DEMout}$ and, assuming ripple and noise are suppressed, K_d for PC1, PC2, and PC3 can be expressed as:

$$K_d(PC1) = V_{CC}/\pi \quad \text{(B1)}$$

$$K_d(PC2) = V_{CC}/2\pi \text{ or } V_{CC}/4\pi \text{ (mode dependent)} \quad \text{(B2)}$$

$$K_d(PC3) = V_{CC}/2\pi \quad \text{(B3)}$$

Equation B2 generally is used in the $V_{CC}/4\pi$ form. In this application report, however, the $V_{CC}/2\pi$ form is used because PC2 is not fully periodic. It is periodic only as long as the phase is changing in one direction. As such, it is sequential, with $V_{CC}/2\pi$ gain. In the PC2 slip mode, there is a similar but opposite phase characteristic to that of PC3. In the PC2 lock mode there is both up and down ranging, but typically from $V_{CC}/2$, giving the $V_{CC}/4\pi$ gain factor.

K_o VCO gain factor expressed in radians/second-V or Hz/V (rad/s is used for brevity) in the text. Where the derivative of phase is frequency:

$$f_{osc} = d\phi/dt = K_o V_c$$

Using Laplace transforms for the complex-frequency domain, $d\phi/dt$ becomes $s\phi(s)$, and $s\phi(s) = K_o V_c(s)$. If an initial condition of $\phi_o(t) = 0$ is assumed at $t = 0$, the VCO gain factor is given by:

$$K_o = s\phi(s)/V_c(s)$$

and the VCO gain is given by:

$$\phi(s)/V_c(s) = K_o/s \quad \text{(B4)}$$

It is important to note that a simplification of the steady-state loop response can be derived from the Laplace-transform final-value theorem, which states that $\lim[\phi(t)] = \lim[s\phi(s)]$, where t goes to infinity as s goes to zero. That is, simplified calculations can be made without transforming back to the time domain.

F(s) Loop-filter transfer function. The order of the loop is determined by the type of filter used. The most common filter and the type discussed in this application report is the second order, as defined by the power of s in the denominator of the complete loop transfer function. Figure 2 shows the simplest filter, with a series R and shunt C. Figure 29 shows the most commonly used filters and gives the transfer functions for each.

$H(s)$ Closed-loop gain. Although the PLL system has limited meaning as an open loop, the open-loop gain elements can be used in a general closed-loop feedback expression to determine the expression for H(s). The open-loop gain, G(s), is given by:

$$G(s) = K_o/s)K_dF(s)$$

and the closed-loop gain H(s) is given by:

$$H(s) = G(s)/[1 + G(s)] = K_oK_d/[s + K_oK_dF(s)] \quad \text{(B5)}$$

$\phi e(s)$ Phase error ($\phi_i - \phi_o$) and is closely related to the closed-loop gain. With $\phi_o(s)/\phi_i(s) = H(s)$ and with manipulation:

$$[\phi_i(s) - \phi_o(s)]/\phi_i(s) = 1 - [\phi_o(s)/\phi_i(s)$$

or

$$\phi e(s) = 1 - H(s) \quad \text{(B6)}$$

This expression with the final-value theorem can lead to a simpler and quicker solution than transforming back to the time domain.

ω_n Natural frequency of the second-order loop from terminology used in earlier feedback and servo theory. It is analogous to ringing frequency in an RLC circuit. Refer to the loop equations in Figure 29 for the values of ω_n.

ζ Damping factor (ratio) of the second-order loop from terminology used in earlier feedback and servo theory. Critical damping occurs for $\zeta = 1$. Refer to the loop equations in Figure 29 for the damping-factor equations.

ω_{3dB} Used to define the conceptual relationship of 3-dB bandwidth for the closed loop. It is determined by setting the squared absolute magnitude of the transfer function $|H(j\omega)|^2 = 0.5$ and solving for ω.

ω_f Used in this application report to define the bandwidth of the loop filter, as a simpler approach to finding the time-constant values.

ω_p Pull-in or capture range. Pull-in range identifies the frequency range over which the PLL can snap into lock without further cycle slipping, assuming that it was not initially locked and that it reaches lock after slipping cycles.

$\Delta\omega_l$ Lock-in range of the VCO, where lock is established without slipping cycles. (It is also referred to as seize range.)

$\Delta\omega_h$ Hold-in range (also called the tracking range or lock range). It is the frequency range over which lock is maintained, assuming the input frequency is continuous and varying within the hold-in range.

T_p Pull-in time for the loop to establish lock. It extends for more than one cycle.

T_l PLL lock-in time without slipping cycles

T_s Settling time for the VCO to achieve 90% energy at the new frequency

Refer to the *Bibliography and References* section and other text material for more complete information relative to the above definitions. Only the use of the HC/HCT4046A, HC/HCT7046A, and related PLL system parameters are discussed in this application report and appendix.

Appendix C Basic Program for VCO Frequency Calculations

```
REM Program for HC4046A VCO Frequency with & w/o offset
REM Name “PLL.BAS”
REM
Start:
INPUT “Enter center frequency, Fo   “, Fo
INPUT “Enter Offset frequency, Fmin, enter 0 if none  “, Fmin
INPUT “Enter power supply voltage, Vcc (Vdd)   “, Vcc
PRINT “6 pf of stray cap. is assumed, Ctotal = Cstray + C1”
Vramp = (.1*Vcc+.6)–(–.7)
Tpd = EXP (–.434*LOG(Vcc)–17.5)
REM Tpd approx. 12.5 nanoseconds, Vcc=5V
Cs=6E–12 : Rdn=50
IF Fmin > Fo THEN PRINT “bad data, try again”
IF Fmin > Fo THEN Start
IF Fmin > .9 * Fo THEN PRINT “Offset too close to Fo, Poor choice!”
IF Fmin<>0 THEN Offset
REM IF Fmin=0 THEN NoOffset
PRINT “Prop Delay, Tpd = “, Tpd
REM
NoOffset:
REM I1 empirical equation,guestimate
I1=EXP(.45*LOG(Fo)–15)
REM MI equation from graph fit
Ml=–.04343*LOG(I1/.001)+6
Isum=M1*I1
R1=Vcc/(2*I1)
REM if Ct selected as initial data, est. with this
REM Ct=EXP(–.667*LOG(Fo)–13.196)
REM C1 values less than 40 pF should not be used
REM IF Ct<4.6E–11 THEN Ct=4.6E–11
Tc=((1/Fo)–2*Tpd)/2
Ct=Tc*Isum/(Vramp–(Isum*Rdn))
Cl=Ct–Cs
PRINT “RI = “, R1
PRINT “C1 = “, C1
PRINT “I1 = “, I1
PRINT “M1 = “, M1
PRINT “Isum = “, Isum
PRINT
INPUT “Pick preferred numbers for R1,C1 & plot Fvco? y/n?  “, Q1$
IF Q1$ = “n” THEN Quit
RepeatNoOffset:
INPUT “New C1 = “, C1
INPUT “New R1 = “, R1
PRINT “Vcoin(V)  ”,” Fvco(Hz) “
“FOR Vcoin=1 TO Vcc–.5 STEP .5
I1=Vcoin/R1
Isum=(–.04343*LOG(I1/.001)+6)*I1
Tc=(C1+Cs)*(Vramp–Isum*Rdn)/Isum
Fvco=l/(2*Tpd+2*Tc)
IF Vcoin=(Vcc/2)–.5 THEN Fl=Fvco
```

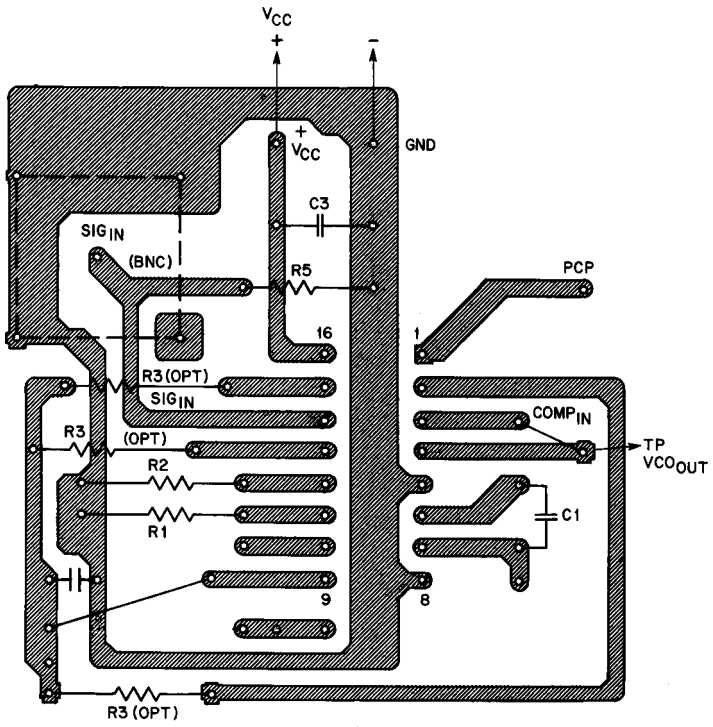
```
IF Vcoin=(Vcc/2)+.5 THEN Fh=Fvco
Ko=((Fh–Fl)/1)*2*3.14159
PRINT  Vcoin, Fvco
NEXT
PRINT
PRINT “Ko = “, Ko , “radians/V”
PRINT
INPUT “Repeat preferred number calc. for R1,C1? y/n? “, Q2$
IF Q2$ = “y” THEN RepeatNoOffset ELSE Quit
REM
Offset:
REM empirical guestimate
I2=EXP(.45*LOG(Fmin)–15)
R2=(Vcc–.6)/I2
M2=–.087*LOG(I2)+4.6+.4*Voc
Tcmin=((1/Fmin)–2*Tpd)/2
Ct=Tcmin*M2*I2/(Vramp–M2*I2*Rdn)
C1=Ct–Cs
Tco=((1/Fo)–2*Tpd)/2
Isum=Ct*Vramp/(Tco+Ct*Rdn)
M1I1=Isum–M2*I2
REM empirical equation for I1 based on given M1*I1 vs I1
I1=EXP(1.007113*LOG(M1I1)–1.755368)
M1=M1I1/I1
R1=(Vcc/2)/I1
PRINT “R1 = “, R1
PRINT “R2 = “, R2
PRINT “C1 = “, C1
PRINT “I1 = “, I1
PRINT “I2 = “, I2
PRINT “M1 = “, M1
PRINT “M2 = “, M2
PRINT “Isum = “, Isum
INPUT “Pick preferred numbers for Fvco vs Vcoin plot?  y/n? “, Q3$
IF Q3$=”n” THEN Quit
PRINT “Note. IN NO CASE SHOULD Rl OR R2 BE LESS THAN 3000 Ω!!”
RepeatOffset:
INPUT “Enter preferred value of C1  “, C1
INPUT “Enter preferred value of R1  “, R1
INPUT “Enter preferred value of R2  “, R2
PRINT “Vcoin”, “Fvco”, “Isum”
FOR Vcoin = 1 TO Vcc–.5 STEP .5
I2=(Vcc–.6)/R2
I1=Vcoin/Rl
Ml=–.04343*LOG(I1/.001)+6
M2=–.087*LOG(I2)+4.6+.4*Vcc
Isum=M1*I1+M2*I2
Tc=((C1+Cs)*(Vramp–Isum*Rdn))/Isum
Fvco=l/(2*Tc+2*Tpd)
IF Vcoin=(Vcc/2)–.5 THEN Fl=Fvco
IF Vcoin=(Vcc/2)+.5 THEN Fh=Fvco
Ko=((Fh–Fl)/1)*2*3.14159
PRINT Vcoin, Fvco, Isum
```

```
NEXT
PRINT
PRINT “Ko = “, Ko, “ radians/volt ”
PRINT
INPUT “Try other preferred values?  y/n? “, Q4$
IF Q4$ = “y” THEN RepeatOffset ELSE Quit
REM
Quit:
END
```

Appendix D R_1, R_2, and C_1 Values With Calculated f_{osc} PC Solutions From Equations 3, 4, and 5 (V_{CC} = 6 V)

EXAMPLE	R_1 (kΩ)	R_2 (kΩ)	C_2	VCO_{in} (V)	CALCULATED (PC) f_{osc}	ERROR (%)	APPROXIMATE (RULE-OF-THUMB EQUATION) f_{osc}	ERROR (%)	MEASURED DATA f_{osc}
1	2000	–	0.084 µF	1	9.9 Hz	28.5	11 Hz	70	7.7 Hz
2	43	–	40 pF	5	3.76 MHz	–17.4	5.37 MHz	18	4.55 MHz
3	8.6	–	40 pF	1	3.77 MHz	19	5.38 MHz	70	3.17 MHz
4	6.2	–	220 pF	5	5.63 MHz	12.6	6.8 MHz	36	5.0 MHz
5	20.9	–	40 pF	5	7.19 MHz	–7.8	11.0 MHz	41	7.8 MHz
6	30	82	0.016 µF	0	8.6 kHz	–10.4	7.6 kHz	–20.8	9.6 kHz
7	30	82	0.016 µF	5	31.2 kHz	–19	28.5 kHz	–26	38.5 kHz
8	8.2	8.6	0.15 µF	0	8.6 kHz	–10.4	7.6 kHz	–20.8	9.6 kHz
9	8.2	8.6	0.15 µF	5	22.9 kHz	17.4	15.9 kHz	–18.5	19.5 kHz

Appendix E HC4046A PLL Layout With Simple RC Filter (R_3C_2)



NOTES: A. Remove pin 2 metal if PC3 not used.
B. Use one R3 choice.
C. Bottom view (one layer)

Figure E–1. HC4046A PLL Layout With Simple RC Filter (R_3C_2)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265